

Project Name : C14CR

Platform : Ivy Bridge(PROCESSOR)+Panther Point(PCH)

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23. EC IT8500BX/BIOS/KB CONN

24. CRT/LVDS/PWR SW

25. HDD/ODD /MINI CARD

26. LAN/CARD READER/15DB/JMC251

27. CODEC(ALC269Q)/INT MIC/SPKR

28. EXT_MIC/FingerPrint/USB/FAN/G-SENSOR/Q-key

29. DC IN/MDC/BT/D-Resistor

30. CPU CORE (ISL95831)

31. CPU VCCSA

32. +1.05V(OZ8116)/+0.75VS/+1.8V

33. +1.5VS/+5VA (OZ815)

34. BATT IN/CHARGER(OZ8602)

35. iGPU Core(ISL95831)

36. TP/LED/WEBCAM/USB CHARGER/RS-232 CON

37. VCC SW/+3.3VA/HIGH-SPEED CAP

38. USB 3.0

39. Reseved

40. History

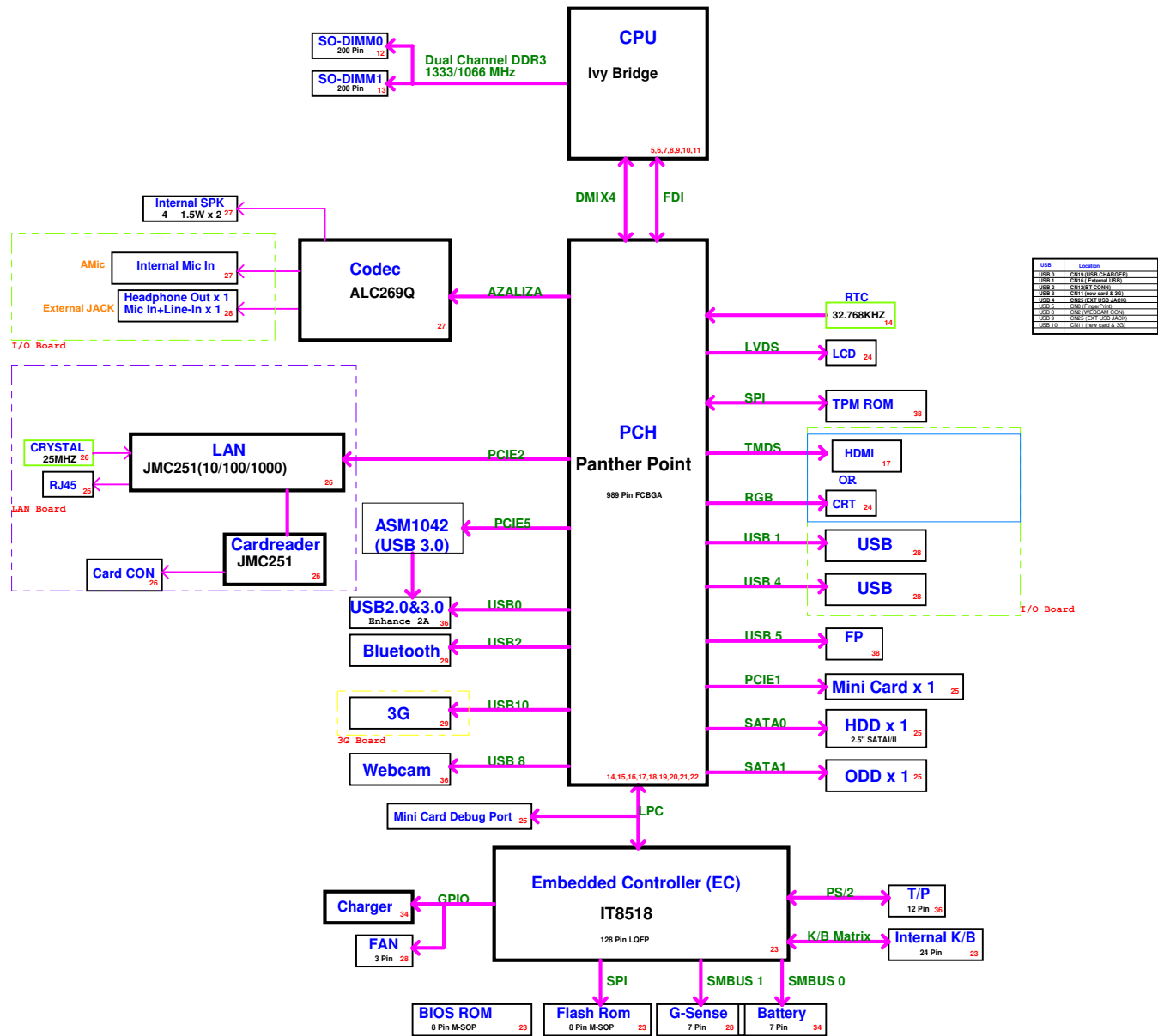
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note
2011/10/24	A	71R-C14CR6-T80A	Motherboard,C14CR0X,189.8*202*1.2mm, 2pcs,6L,Ver.A,TTL,	6BR-C14CR0-000A	
2011/12/06	B	71R-C14CR6-T80B	Motherboard,C14CR0X,189.8*202*1.2mm, 2, 6L,Rev.B,TTL,	6BR-C14CR0-000B	

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

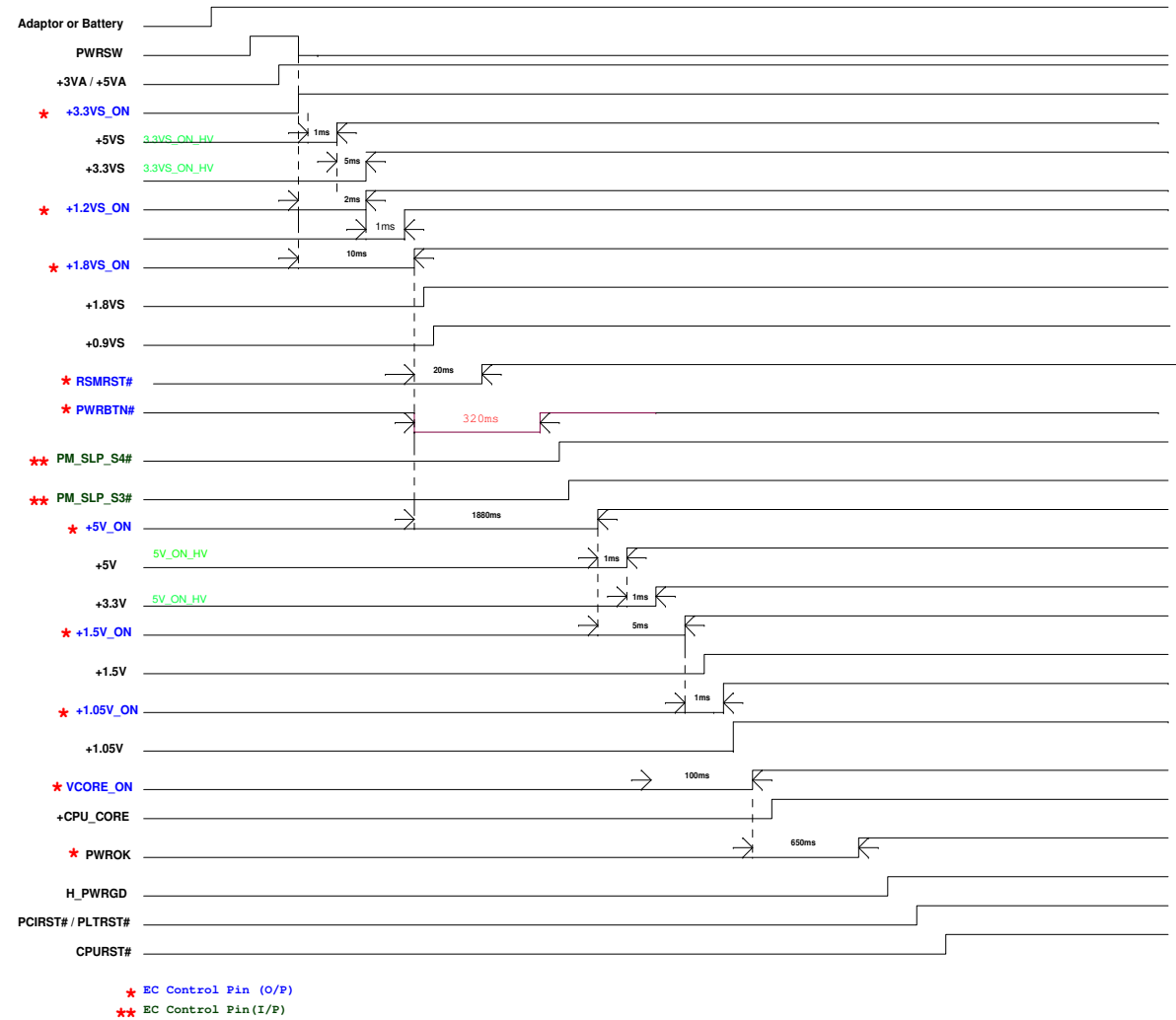
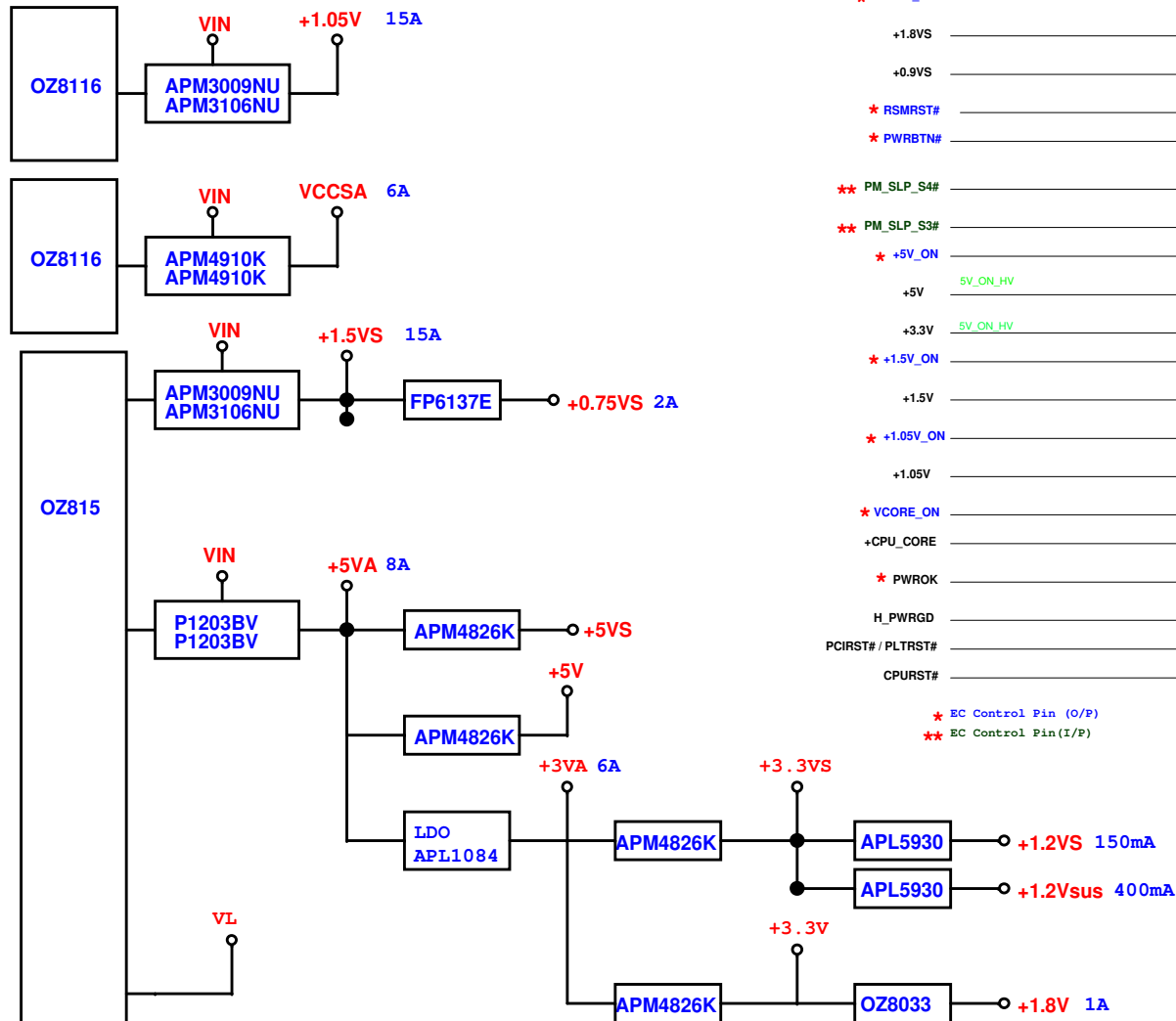
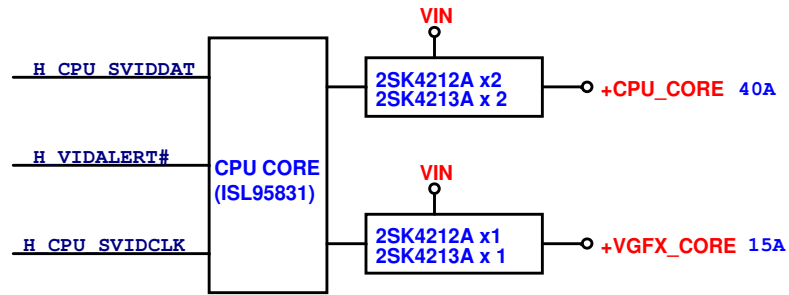
SYSTEM BLOCK DIAGRAM



USB	Location
USB 0	CH1 USB (CHARGER)
USB 1	CH1 USB (External USB)
USB 2	CH1 USB (Cable)
USB 3	CH1 USB (USB 3.0)
USB 4	CH1 USB (USB 3.0)
USB 5	CH1 USB (USB 3.0)
USB 6	CH1 USB (USB 3.0)
USB 7	CH1 USB (USB 3.0)
USB 8	CH1 USB (USB 3.0)
USB 9	CH1 USB (USB 3.0)
USB 10	CH1 USB (USB 3.0)

POWER BLOCK DIAGRAM

System Poewr On Sequence



Panther Point GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	N.C (TACH3)
GPIO8	N.C
GPIO9	N.C (WOL_EN)
GPIO10	N.C (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	N.C (GLAN_DOCK#)
GPIO14	N.C (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	N.C (TACH0)
GPIO18	N.C
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	N.C (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	N.C (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8518 GPIO		Default Pull/Mode
GPA0	PID_3_RF_LED_ON#	UP / GPIO
GPA1	BATT_VA_OFF#	UP / GPIO
GPA2	BTL_BEEP	UP / GPIO
GPA3	WLAN_PWR#	UP / GPIO
GPA4	+1.05V_ON	UP / GPIO
GPA5	SENBAT_V	UP / GPIO
GPA6	PM_RSMRST#	UP / GPIO
GPA7	EC_BL_PWM	UP / GPIO
GPB0	PM_SLP_S4#	UP / GPIO
GPB1	PM_SLP_S3#	UP / GPIO
GPB2	3G_PWR#	Dn / GPIO
GPB3	SMBCLK	/ GPIO
GPB4	SMBDAT	/ GPIO
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Func1
GPB7	SAFTY_PROTECT	Dn / GPIO
GPC0	+1.5V_ON	Dn / GPIO
GPC1	SMB_CLK_EC	/ GPIO
GPC2	SMB_DAT_EC	/ GPIO
GPC3	PID_0_CHG_B_LED	Dn / GPIO
GPC4	PWRBTN3#	Dn / GPIO
GPC5	PANEL_DETECT_2	Dn / GPIO
GPC6	VCCSA_ON	Dn / GPIO
GPC7	+1.5VS_ON	UP / GPIO
GPD0	ADAP_IN	UP / GPIO
GPD1	PWRBTN#	UP / GPIO
GPD2	PLT_RST#	UP / Func1
GPD3	PM_SUS_STAT#	UP / GPIO
GPD4	EC_EXTSMI#	UP / GPIO
GPD5	Fastcharge_EN	UP / GPIO
GPD6	+5V_ON	Dn / GPIO
GPD7	SET_V	Dn / GPIO
GPE0	LID#	Dn / GPIO
GPE1	PWR_USB_LED	Dn / GPIO
GPE2	ALL_SYS_PGD	Dn / GPIO
GPE3	Vcore_ON	Dn / GPIO
GPE4	PWRSW	UP / GPIO
GPE5	LVDS_VIN	Dn / GPIO
GPE6	WLAN_ON	Dn / GPIO
GPE7	AMP_MUTE#	UP / GPIO
GPF0	PCH_BL_EN	UP / GPIO
GPF1	+1.8V_ON	UP / GPIO
GPF2	BT_ON	UP / GPIO
GPF3	N.C	UP / GPIO
GPF4	TP_CLK	UP / GPIO
GPF5	TP_DATA	UP / GPIO
GPF6	EC PECl	UP / GPIO
GPF7	CHG_HI VOLT#	UP / GPIO
GPG0	PWRBTN2#	Dn/ GPO/TM
GPG1	+3.3VS_ON	Dn/ GPO/ID7
GPG2	EC PORST	
GPG6	WEBCAN_ON	Dn / GPIO
GPH0	PM_CLKRUN#	Dn/ GPIO/ID0
GPH1	PID_1_CHG_R_LED	Dn/ GPIO/ID1
GPH2	PID_2_PWR_LED	Dn/ GPIO/ID2
GPH3	EC_HSCS0#	Dn/ GPIO/ID3
GPH4	EC_HSCK	Dn/ GPIO/ID4
GPH5	EC_HMISO	Dn/ GPIO/ID5
GPH6	EC_HMOSI	Dn/ GPIO/ID6

ITE8518 GPIO		Default Pull/Mode
GPIO	CRT_DETECT	/ GPIO/ADC
GPJ1	PANEL_DETECT	/ GPIO/ADC
GPJ2	PLATFORM_ID	/ GPIO/ADC
GPJ3	CPPE#	/ GPIO/ADC
GPJ4	BAT_I	/ GPIO/ADC
GPJ5	BATT_TEMP	/ GPIO/ADC
GPJ6	ADAPTOR_1	/ GPIO/ADC
GPJ7	BAT_V	/ GPIO/ADC
GPJ0	EC_BL_ON	/ GPIO/DAC
GPJ1	EC_PROCHOT	/ GPIO/DAC
GPJ2	FAN_CTRL0	/ GPIO/DAC
GPJ3	CHG_REF	/ GPIO/DAC
GPJ4	CHG_I	/ GPIO/DAC
GPJ5	PWR_USB#	/ GPIO/DAC

Ivy Bridge CPU				
	CPU CORE (V)	ICC (A)	W	TEMP ()
IMVP-7	1.05	44.0	36	

Panther Point			
VCC	ICC (mA)	W	TEMP ()
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

Panther Point			
VCC	ICC (mA)	mW	TEMP ()
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

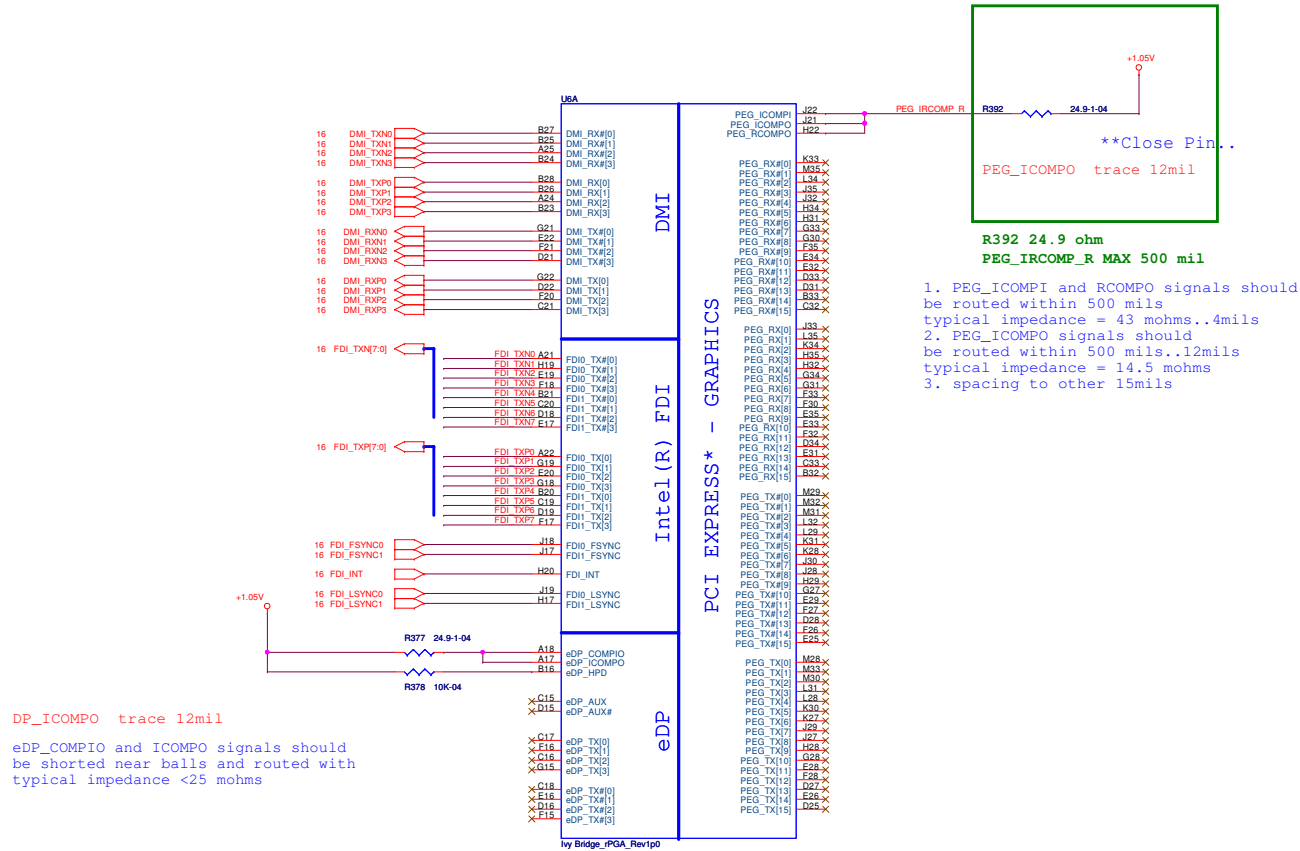
ITE8518			
VCC	ICC (mA)	mW	TEMP ()
+3.3V	100	330	70

IDT92HD87B			
VCC	ICC (mA)	mW	TEMP ()
+3.3V (DVDD)	200	660	70
+5V (AVDD)	1000	5000	

ADM1032			
VCC	ICC	mW	TEMP ()
+3.3V	170uA	0.56	150

JMC251			
VCC	ICC (mA)	mW	TEMP ()
+3.3VS	300	990	70
+1.2VS	150	180	

IVY BRIDGE PROCESSOR(DMI,PEG,FDI)



IVY BRIDGE PROCESSOR (CLK, MISC, JTAG)

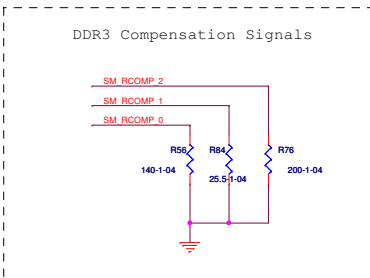
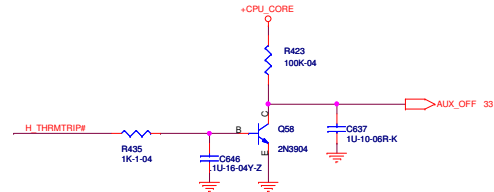
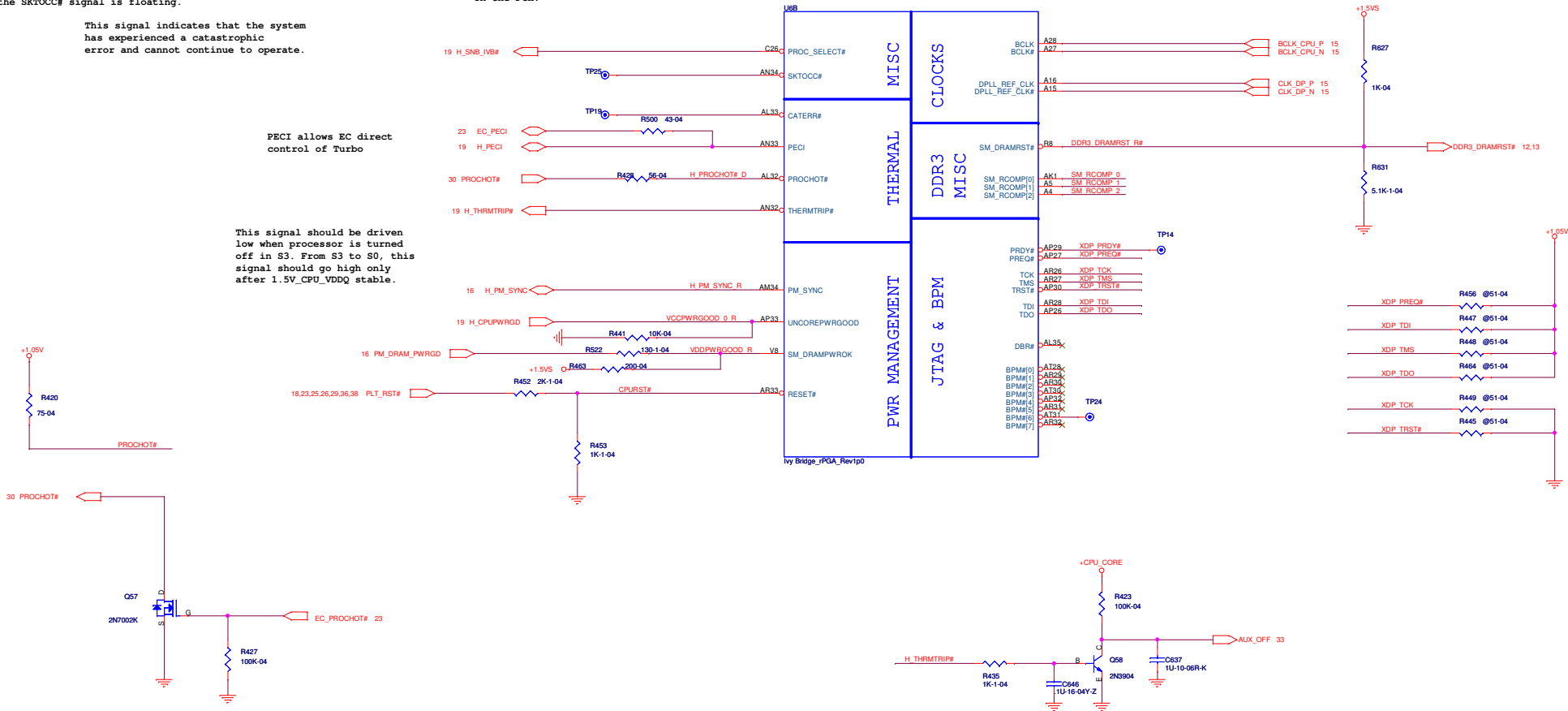
The SKTOCC# pin is driven to ground by the processor when the processor is socketed in the system, otherwise the SKTOCC# signal is floating.

This signal indicates that the system has experienced a catastrophic error and cannot continue to operate.

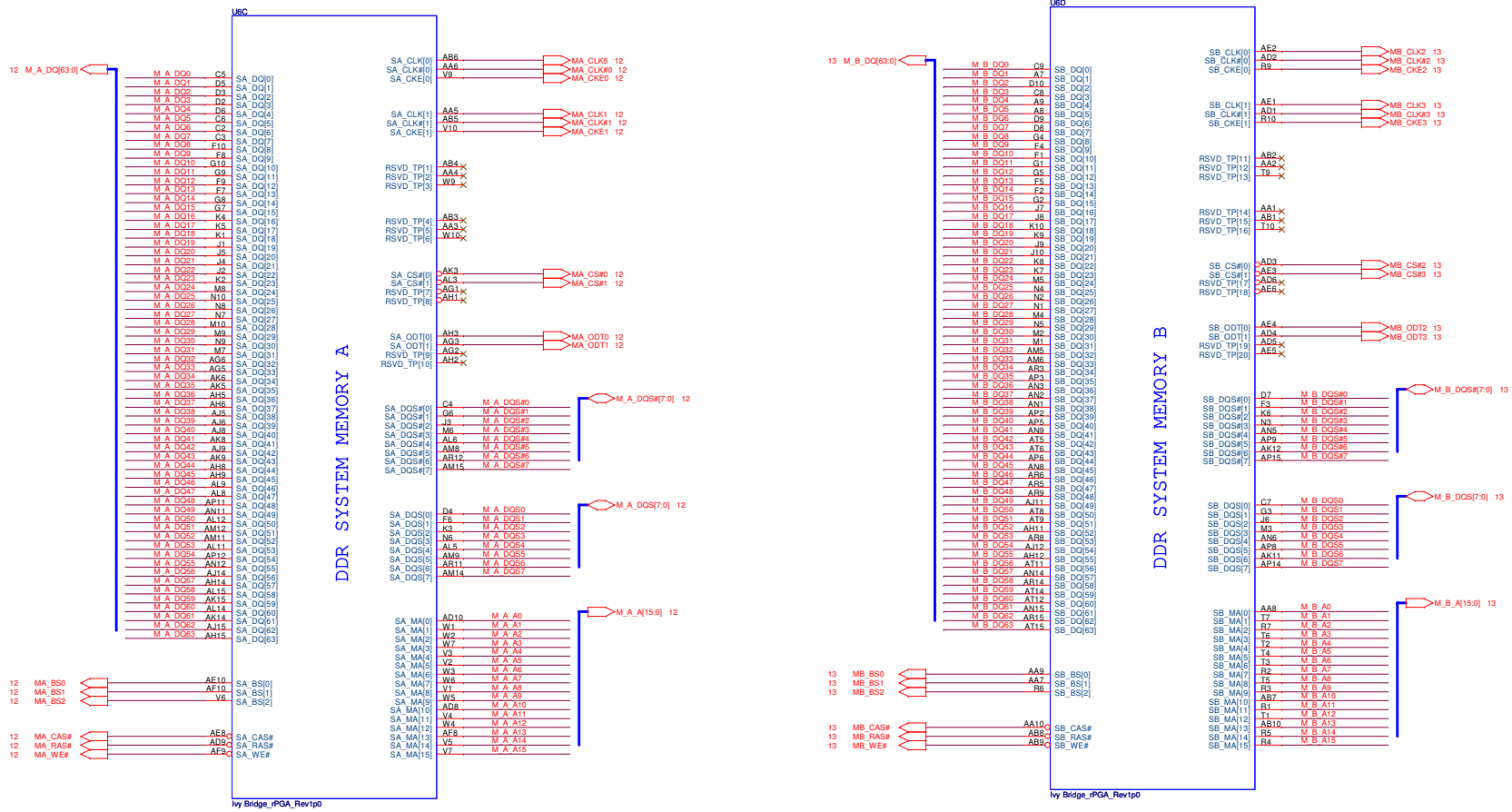
PECI allows EC direct control of Turbo

This signal should be driven low when processor is turned off in S3. From S3 to S0, this signal should go high only after 1.5V_CPU_VDDQ stable.

This pin is for compability with future platforms. A pull up resistor to VCPLL is required if connected to the DF_TVS strap on the PCH.

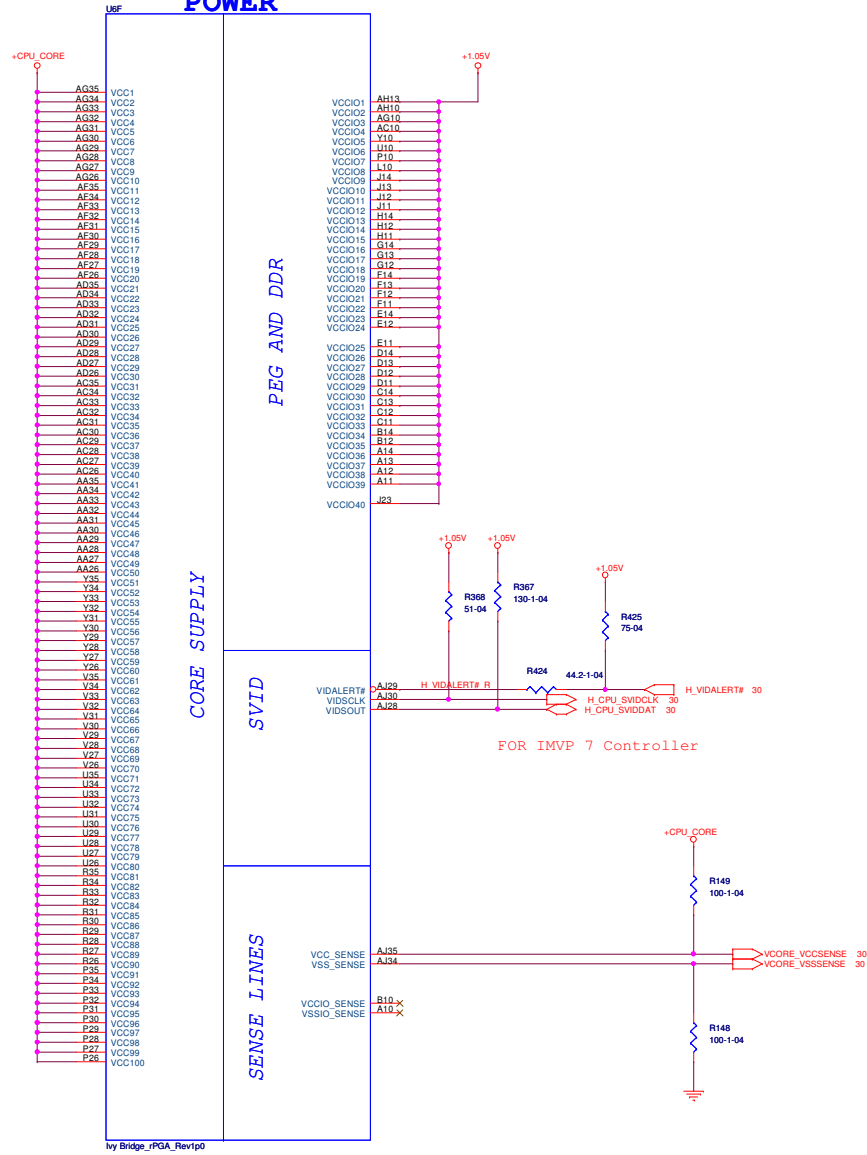


IVY BRIDGE PROCESSOR (DDR3)

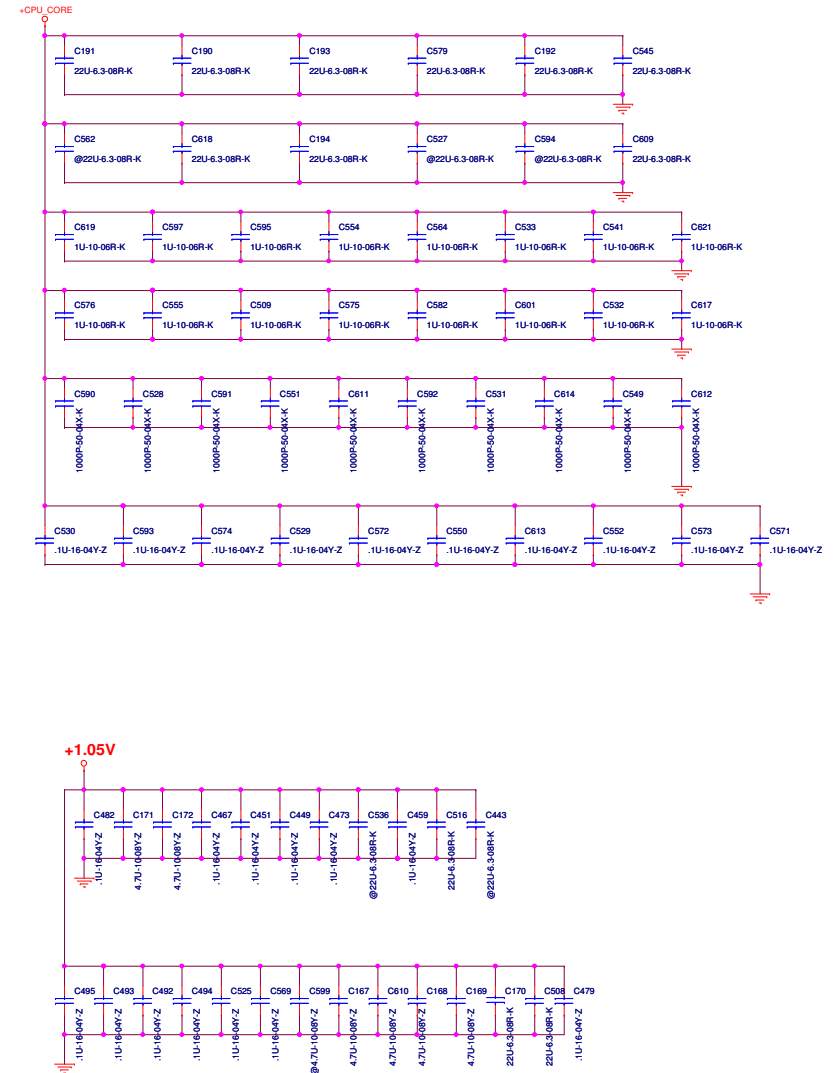


IVY BRIDGE PROCESSOR (POWER)

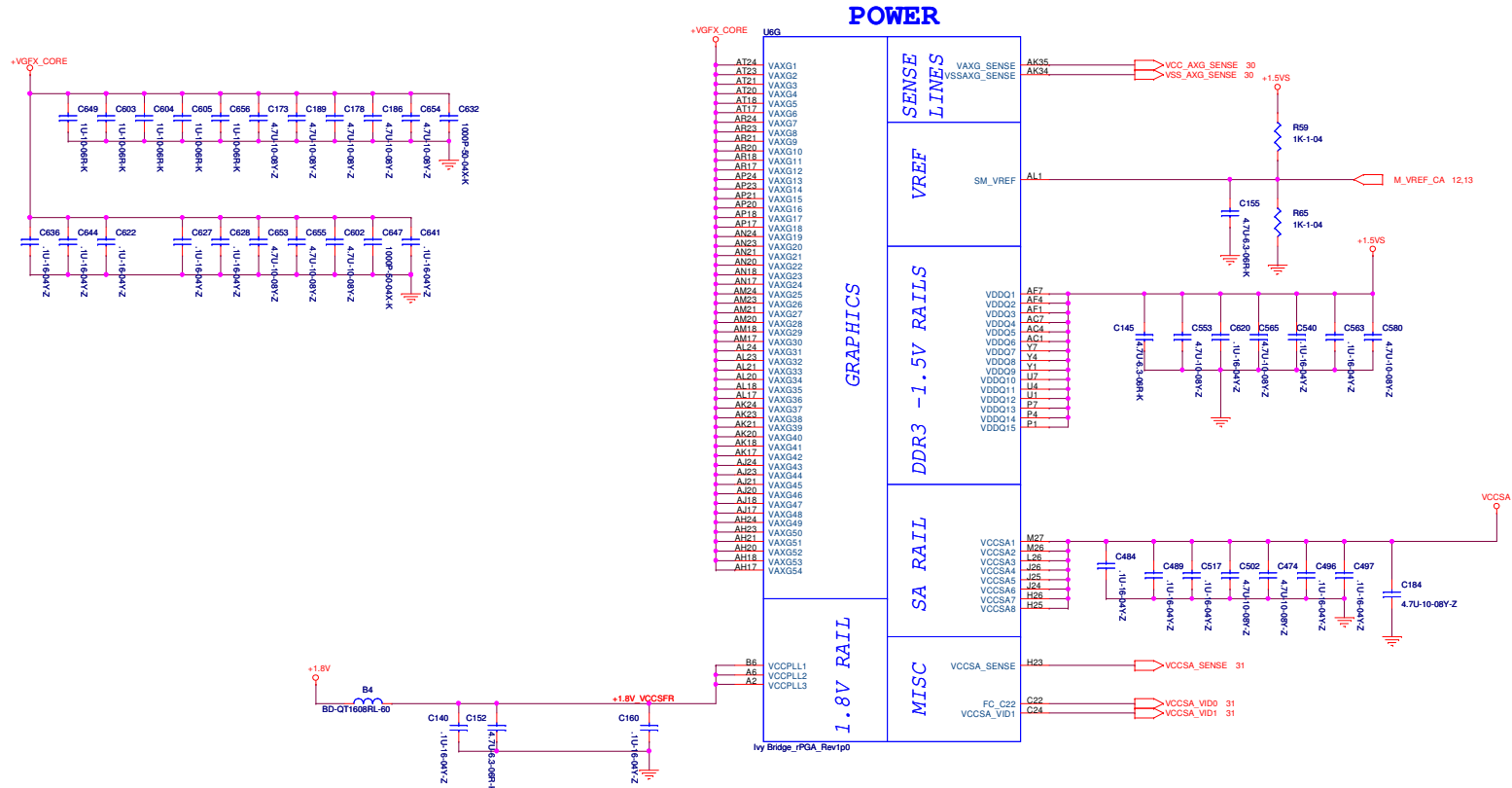
POWER



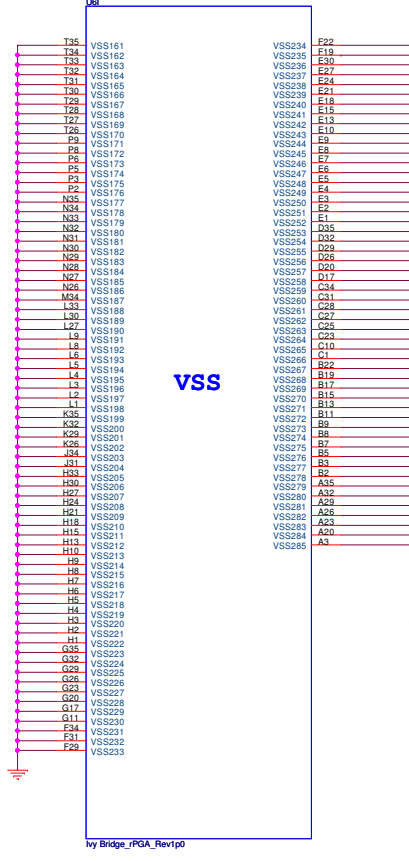
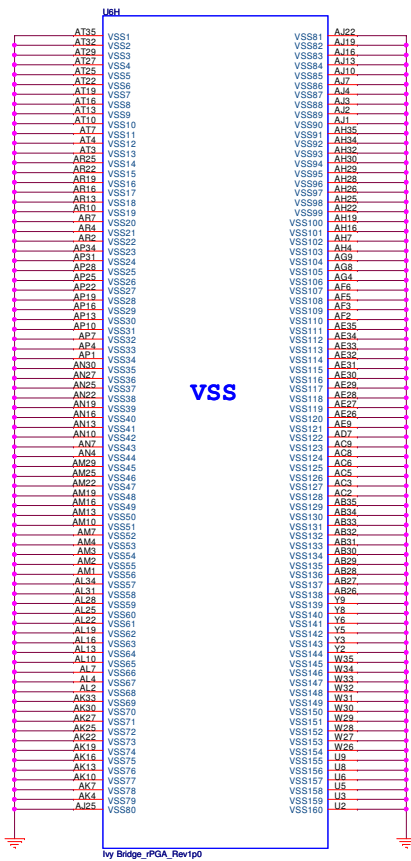
+CPU_Core Decoupling



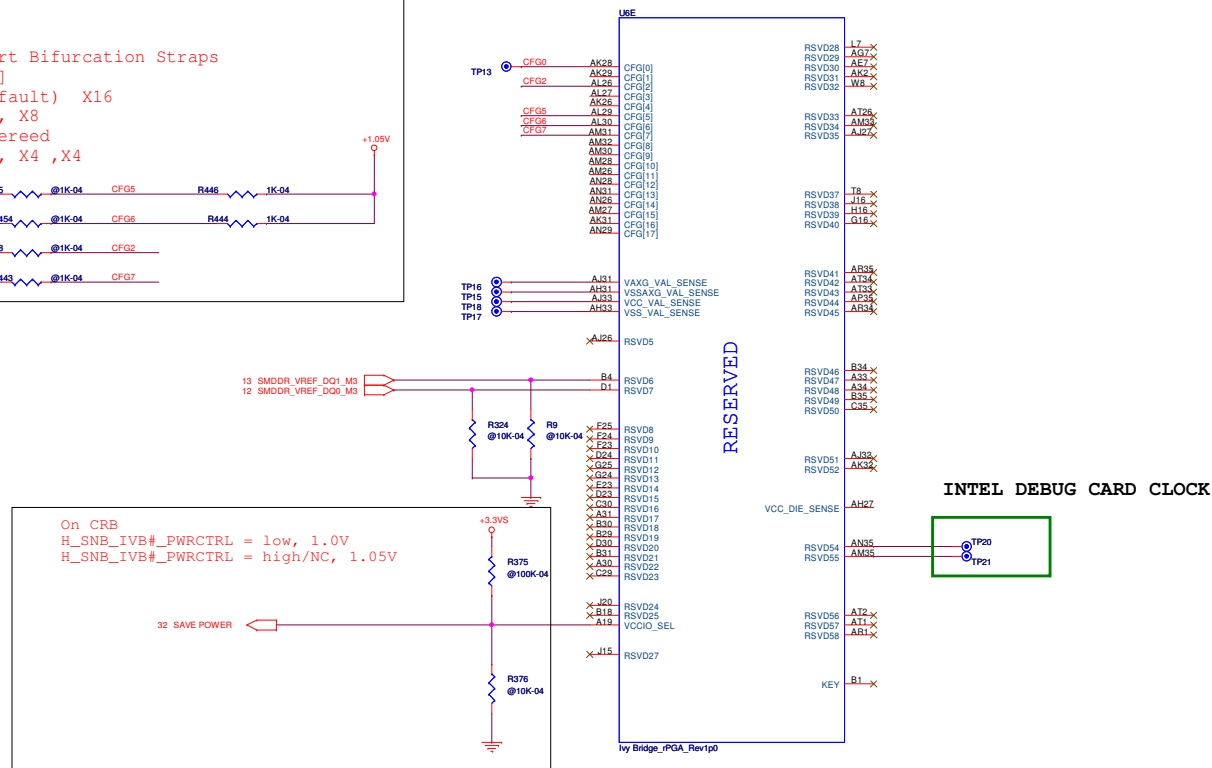
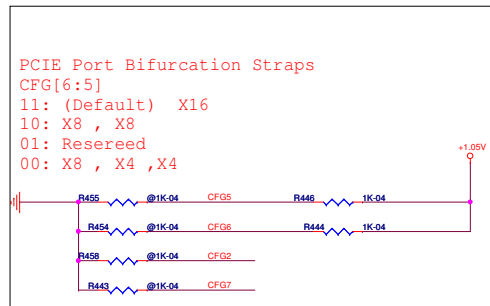
IVY BRIDGE PROCESSOR (POWER)

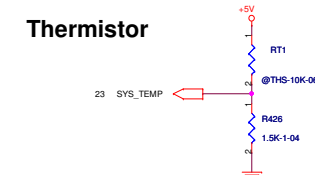


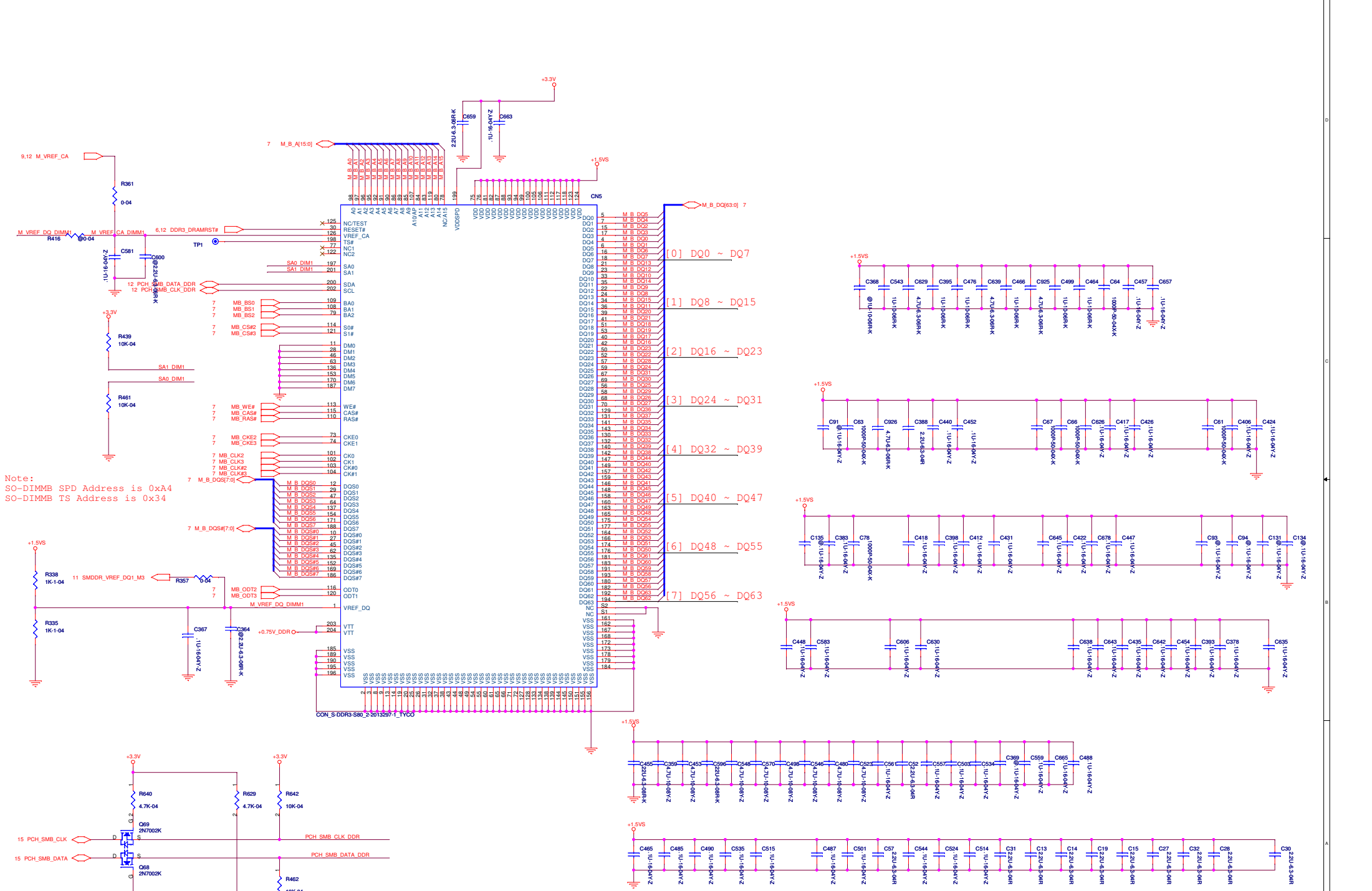
IVY BRIDGE PROCESSOR (VSS)



IVY BRIDGE PROCESSOR (RESERVED)



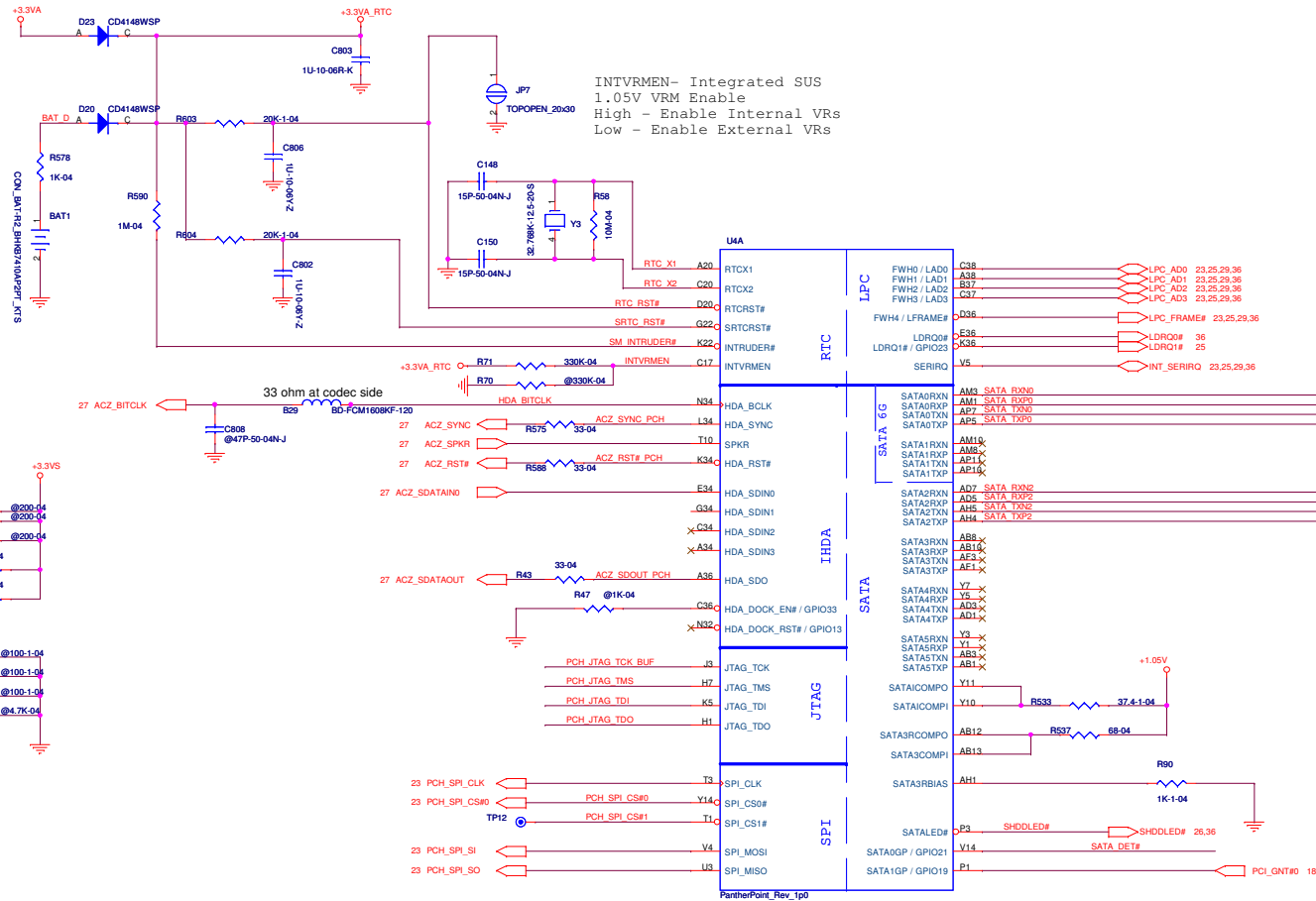




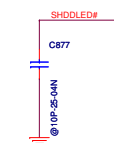
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Panther Point Chipset (RTC,LPC,SATA,HDA,SPI,JTAG)

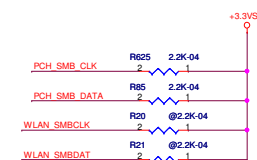
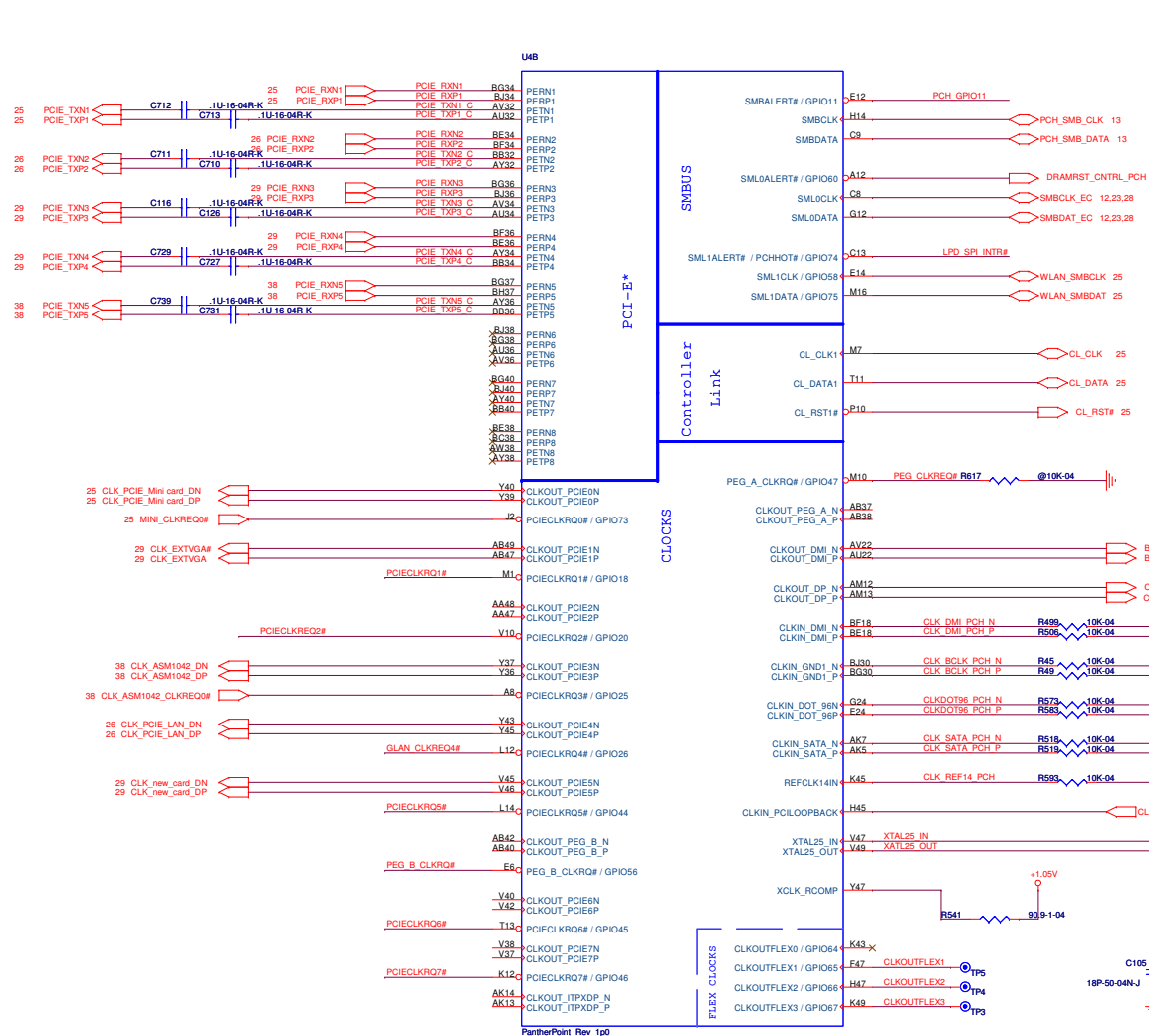
RTC Circuitry



SATA[x]GP pins if unused require 8.2-k to 10-k pull-up to +Vcc3_3 or 8.2-k to 10-k pull-down to ground.

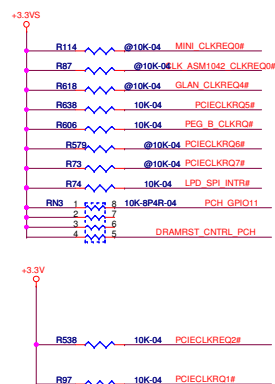


Panther Point Chipset (PCIE,SMBUS,CLOCK)

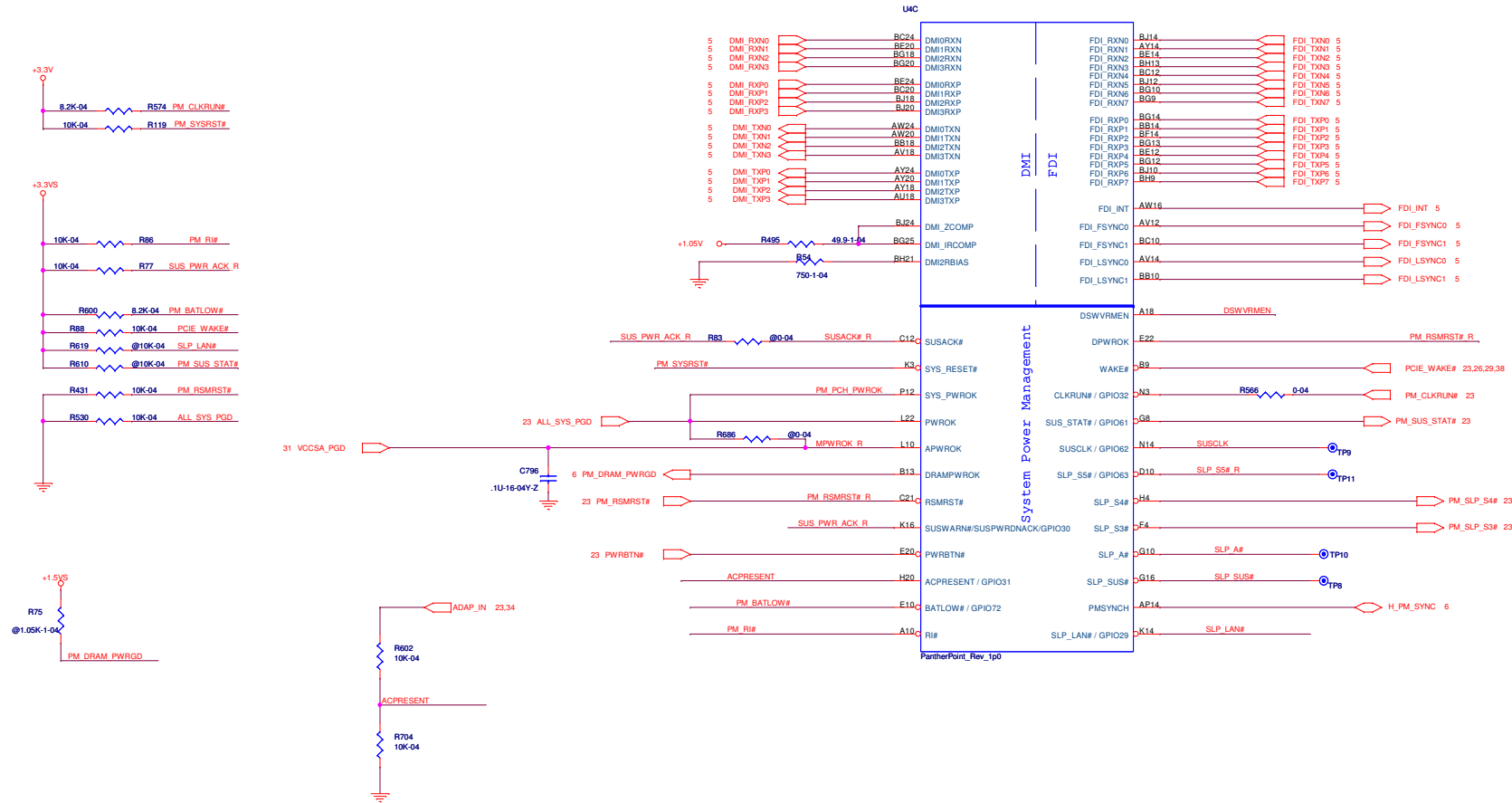


SMB_	DDRA,DDR
SML0_	n/a
SML1_	to EC

This input has to be terminated with a 10-kOhms pull-down termination resistor in Integrated Clock generation mode.



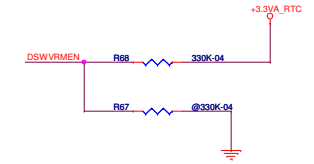
Panther Point Chipset (DMI,FDI)



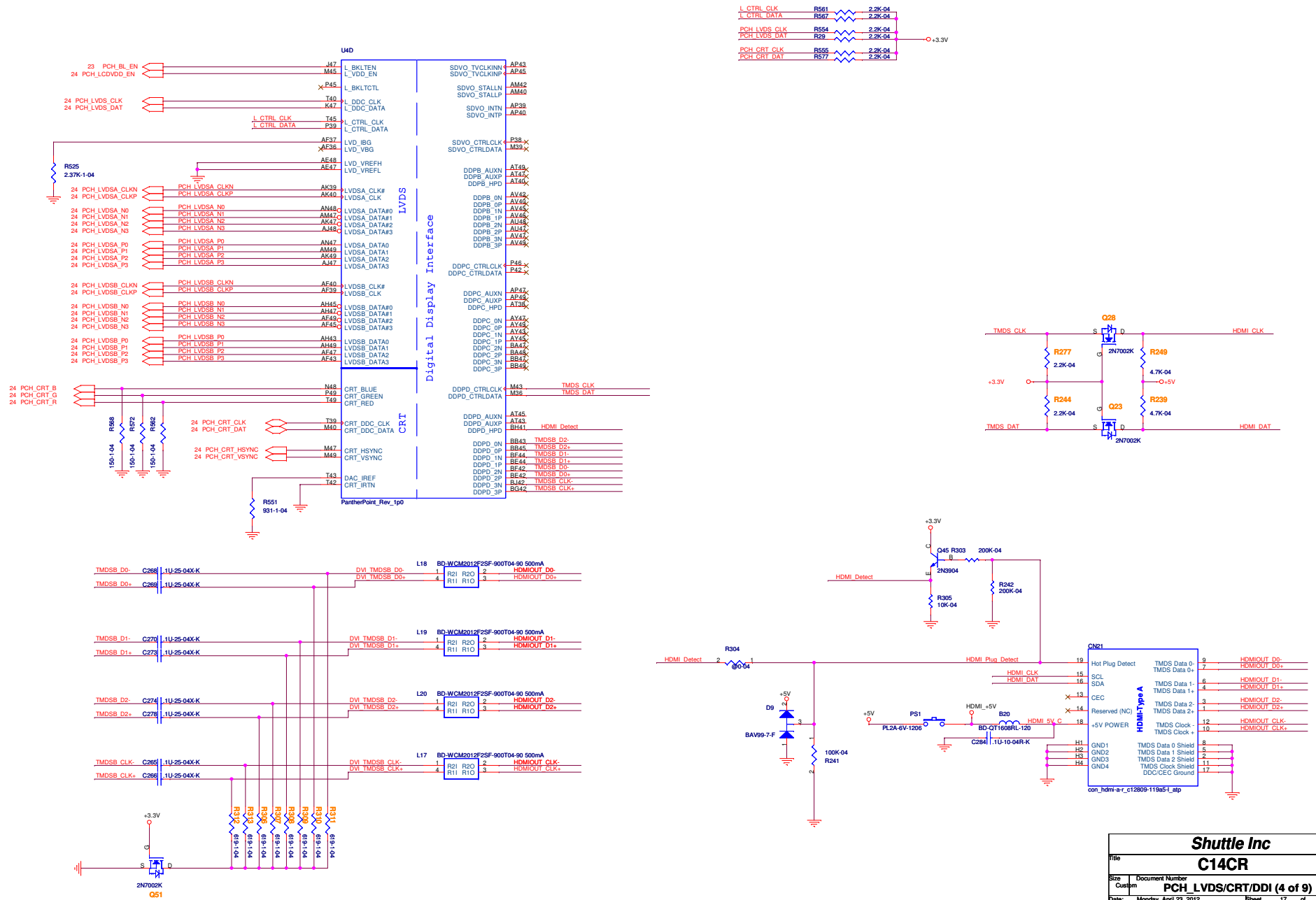
DSWODVREN - On Die DSW VR Enable

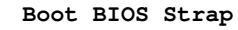
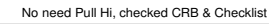
HIGH Enabled (DEFAULT)	Enabled (DEFAULT)
(R132 STUFFED,	
R128 UNSTUFFED	

LOW Disabled
(R128 STUFFED,
R132 UNSTUFFED Disabled



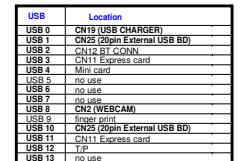
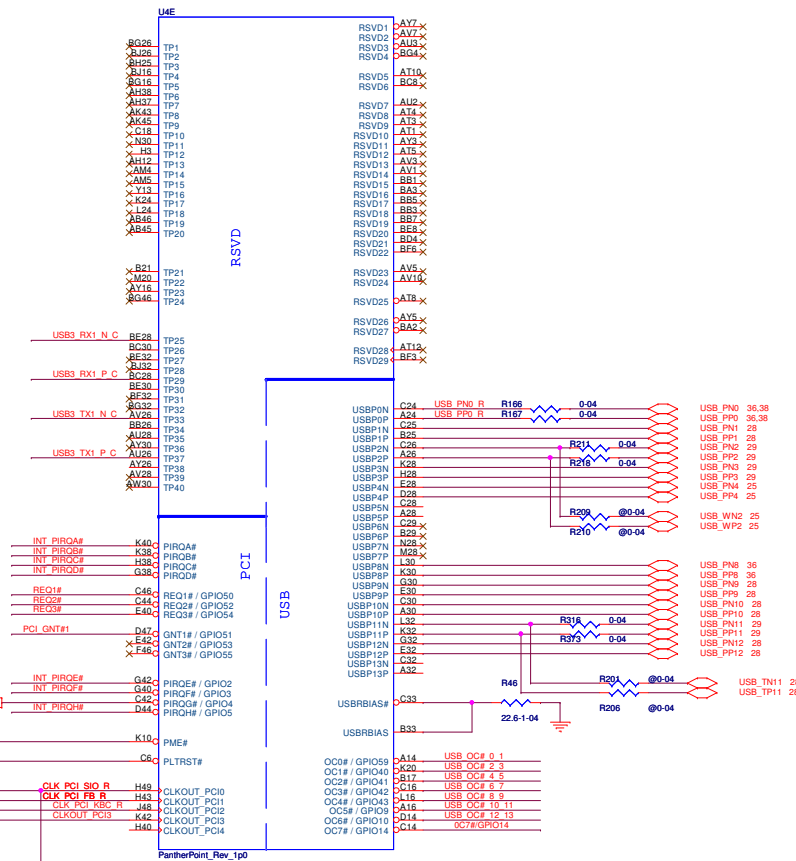
Panther Point Chipset (LVDS,CRT,Digital Display)



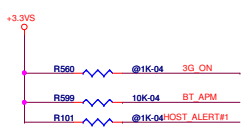
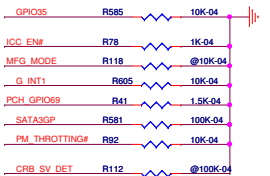
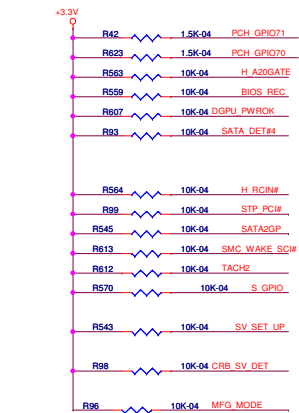


PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
1	1	SPi

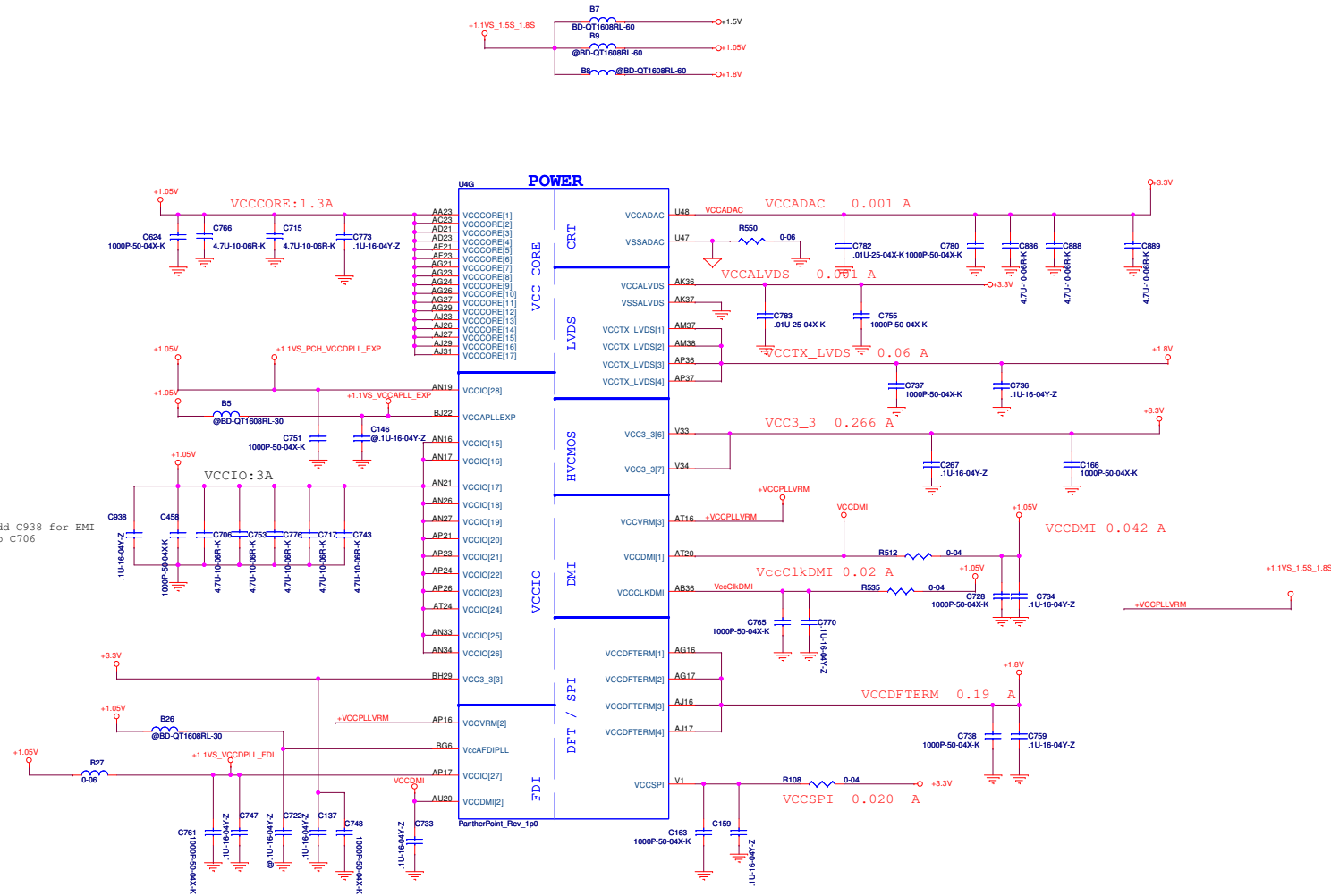
Default

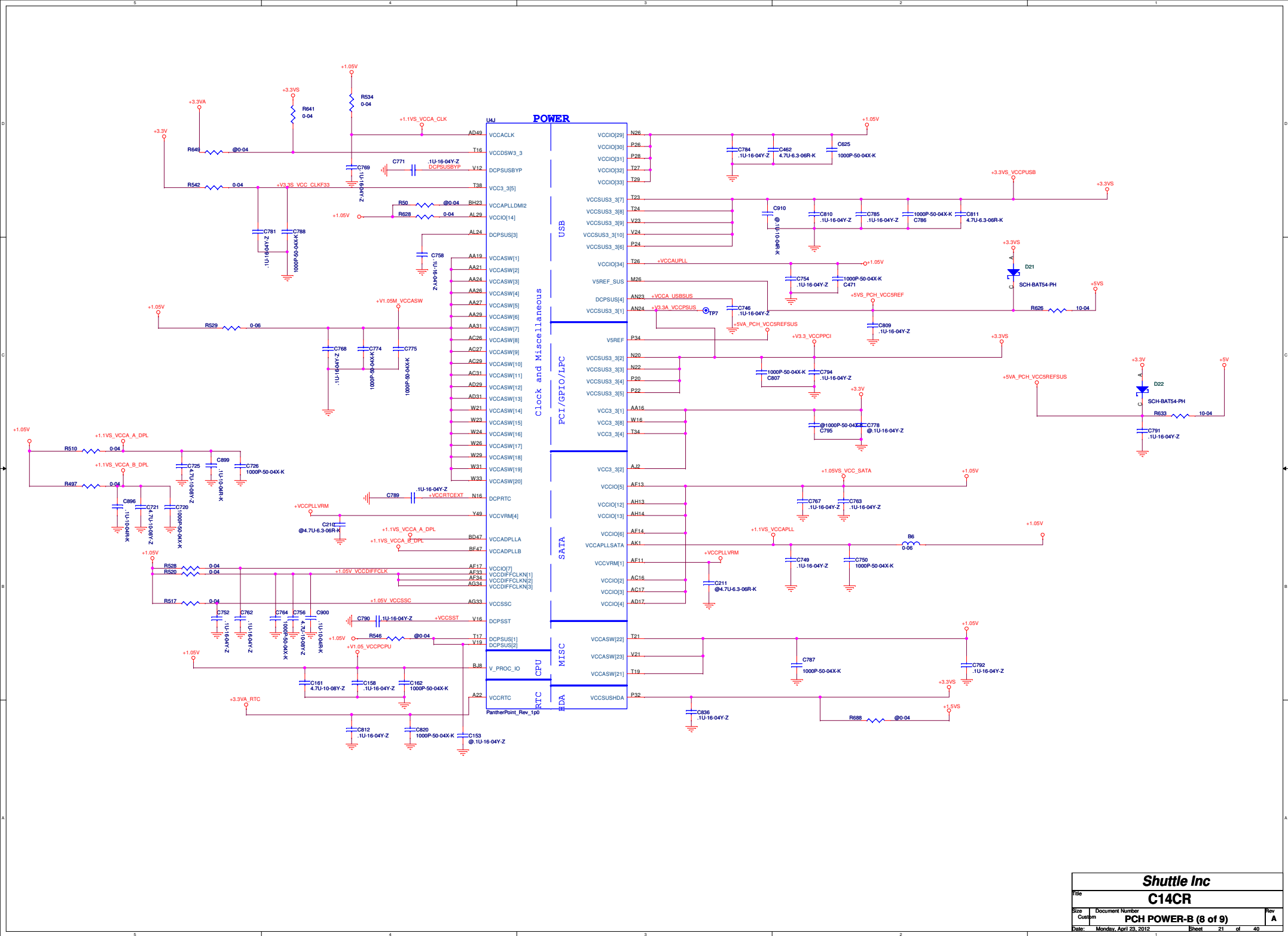


Shuttle Inc			
Title C14CR			
Size	Document Number	Rev	
Custom	PCH_PCI/USB (5 of 9)	A	
Date:	Monday, April 23, 2012	Sheet	18 of 40



11/29 Add C938 for EMI
close to C706



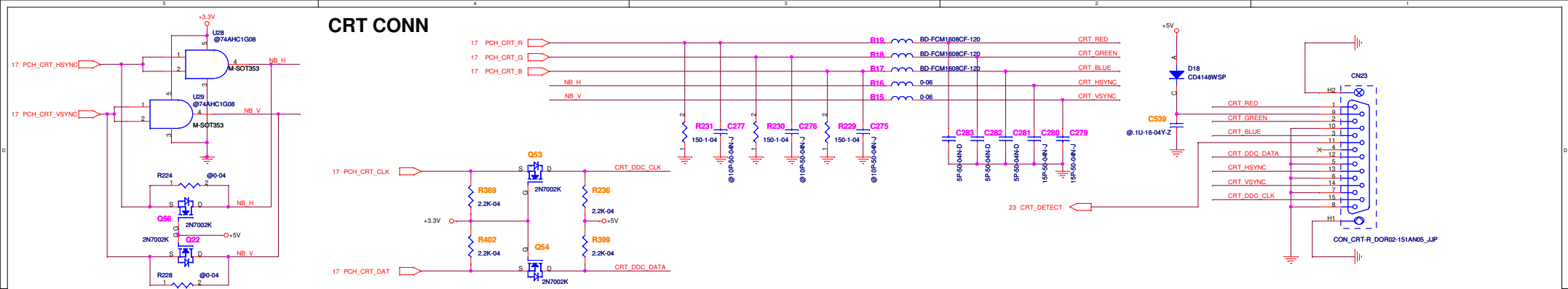


JMH		
H5	VSS[0]	
AA17	VSS[1]	AK38
AA2	VSS[2]	AK4
AA3	VSS[3]	AK42
AA33	VSS[4]	AK46
AA34	VSS[5]	AK8
AB11	VSS[6]	AL16
AB14	VSS[7]	AL17
AB39	VSS[8]	AL19
AB4	VSS[9]	AL2
AB43	VSS[10]	AL21
AB5	VSS[11]	AL23
AB7	VSS[12]	AL25
AC19	VSS[13]	AL27
AC2	VSS[14]	AL31
AC4	VSS[15]	AL33
AC24	VSS[16]	AL34
AC3	VSS[17]	AL46
AC34	VSS[18]	AM11
AC48	VSS[19]	AM14
AD10	VSS[20]	AM36
AD11	VSS[21]	AM38
AD12	VSS[22]	AM43
AD13	VSS[23]	AM45
AD19	VSS[24]	AM46
AD24	VSS[25]	AM7
AD26	VSS[26]	AN2
AD27	VSS[27]	AN29
AD33	VSS[28]	AN3
AD34	VSS[29]	AN31
AD36	VSS[30]	AP12
AD37	VSS[31]	AP19
AD38	VSS[32]	AP28
AD39	VSS[33]	AP30
AD4	VSS[34]	AP32
AD40	VSS[35]	AP38
AD42	VSS[36]	AP4
AD43	VSS[37]	AP42
AD45	VSS[38]	AP46
AD46	VSS[39]	AP8
AD8	VSS[40]	AR2
AE2	VSS[41]	AR48
AE3	VSS[42]	AT11
AE10	VSS[43]	AT12
AE12	VSS[44]	AT18
AD14	VSS[45]	AT22
AD16	VSS[46]	AT26
AE16	VSS[47]	AT28
AF19	VSS[48]	AT30
AF24	VSS[49]	AT32
AF26	VSS[50]	AT34
AF27	VSS[51]	AT39
AF29	VSS[52]	AT42
AF31	VSS[53]	AT46
AF38	VSS[54]	AT7
AF4	VSS[55]	AU24
AF42	VSS[56]	AU30
AF46	VSS[57]	AV16
AF5	VSS[58]	AV20
AF7	VSS[59]	AV24
AF8	VSS[60]	AV30
AG19	VSS[61]	AV38
AG2	VSS[62]	AV4
AG31	VSS[63]	AV43
AG48	VSS[64]	AV8
AH11	VSS[65]	AW14
AH3	VSS[66]	AW18
AH36	VSS[67]	AW2
AH39	VSS[68]	AW22
AH40	VSS[69]	AW28
AH42	VSS[70]	AW28
AH46	VSS[71]	AW32
AH7	VSS[72]	AW34
AJ19	VSS[73]	AW36
AJ21	VSS[74]	AW40
AJ4	VSS[75]	AW48
AJ33	VSS[76]	AV11
AJ34	VSS[77]	AY12
AK12	VSS[78]	AY22
AK3	VSS[79]	AY28

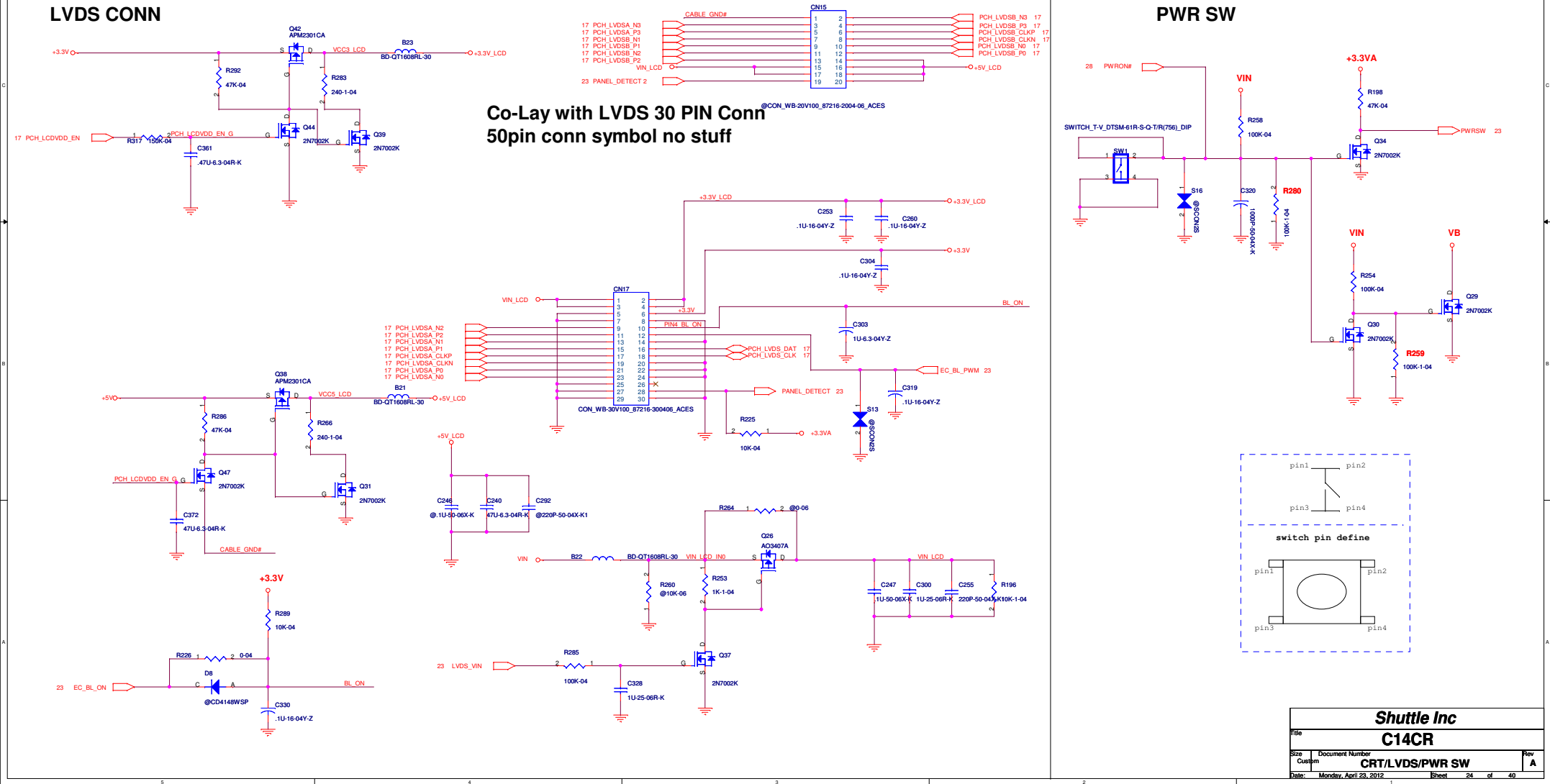
PantherPoint_Rev_1p0

JMI		
AY4	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY6	VSS[162]	K39
B11	VSS[163]	K46
B15	VSS[164]	K7
B19	VSS[165]	L18
B23	VSS[166]	L2
B27	VSS[167]	L20
B31	VSS[168]	L26
B39	VSS[169]	L36
B7	VSS[170]	L46
F45	VSS[171]	M12
BB12	VSS[172]	P16
BB16	VSS[173]	P18
BB24	VSS[174]	M2
BB25	VSS[175]	M22
BB22	VSS[176]	M24
BB24	VSS[177]	M30
BB28	VSS[178]	M32
BB30	VSS[179]	M34
BB36	VSS[180]	M38
BB4	VSS[181]	M4
BB46	VSS[182]	M42
BC14	VSS[183]	M46
BC18	VSS[184]	M8
BC2	VSS[185]	N18
BC22	VSS[186]	P30
BC26	VSS[187]	N47
BC35	VSS[188]	P11
BC34	VSS[189]	P18
BC40	VSS[190]	P40
BC42	VSS[191]	T33
BC46	VSS[192]	P42
BD46	VSS[193]	P7
BD4	VSS[194]	P2
BE22	VSS[195]	P48
BE26	VSS[196]	T12
BE28	VSS[197]	T31
BE10	VSS[198]	T37
BE12	VSS[199]	T4
BE14	VSS[200]	W34
BF20	VSS[201]	T47
BF22	VSS[202]	T48
BF24	VSS[203]	T8
BF26	VSS[204]	V31
BF28	VSS[205]	V11
BF30	VSS[206]	V17
BF32	VSS[207]	V26
BF34	VSS[208]	V27
BF36	VSS[209]	V29
BF40	VSS[210]	V31
BF4	VSS[211]	V36
BG17	VSS[212]	V39
BG21	VSS[213]	V43
BG33	VSS[214]	V7
BG44	VSS[215]	W17
BG8	VSS[216]	W19
BH11	VSS[217]	W2
BH15	VSS[218]	W27
BH17	VSS[219]	W48
BH19	VSS[220]	Y12
H10	VSS[221]	Y38
BH27	VSS[222]	Y4
BH31	VSS[223]	Y42
BH33	VSS[224]	Y46
BH35	VSS[225]	Y8
BH39	VSS[226]	BG29
BH43	VSS[227]	N24
BH7	VSS[228]	AJ3
D3	VSS[229]	AD47
D12	VSS[230]	B43
D16	VSS[231]	BE10
D22	VSS[232]	BG41
D24	VSS[233]	G14
D26	VSS[234]	H16
D28	VSS[235]	T36
D30	VSS[236]	BG22
D32	VSS[237]	BG24
D34	VSS[238]	C22
D36	VSS[239]	AP13
D42	VSS[240]	M14
D6	VSS[241]	AP3
E18	VSS[242]	AP7
E26	VSS[243]	BE16
G18	VSS[244]	BC16
G20	VSS[245]	BG28
G26	VSS[246]	BJ28
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

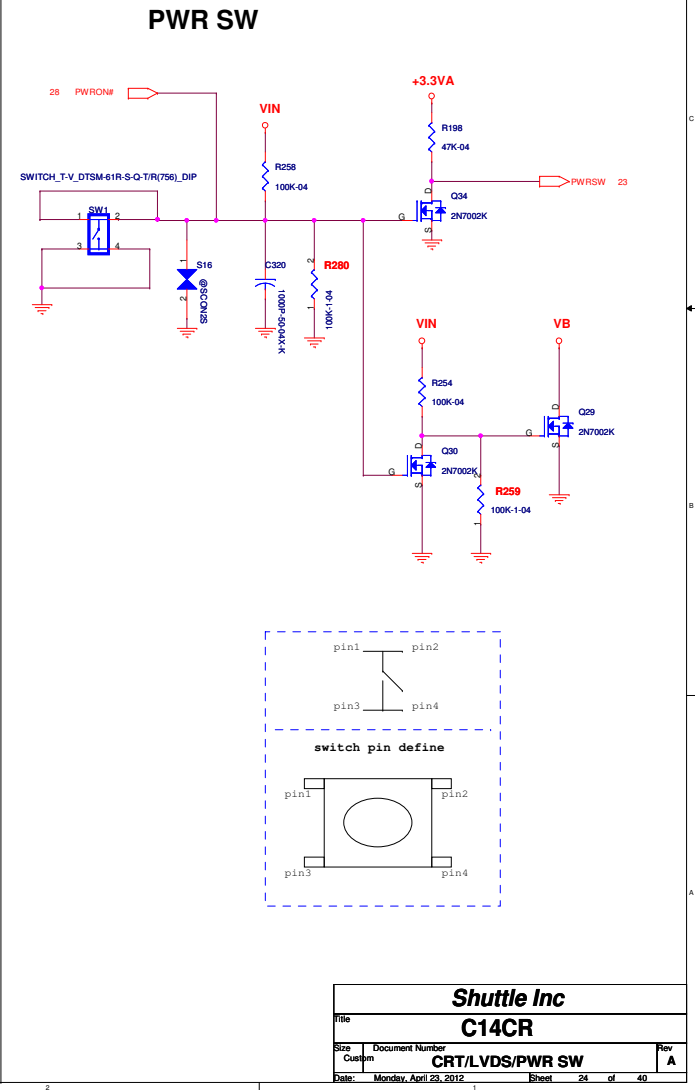
PantherPoint_Rev_1p0

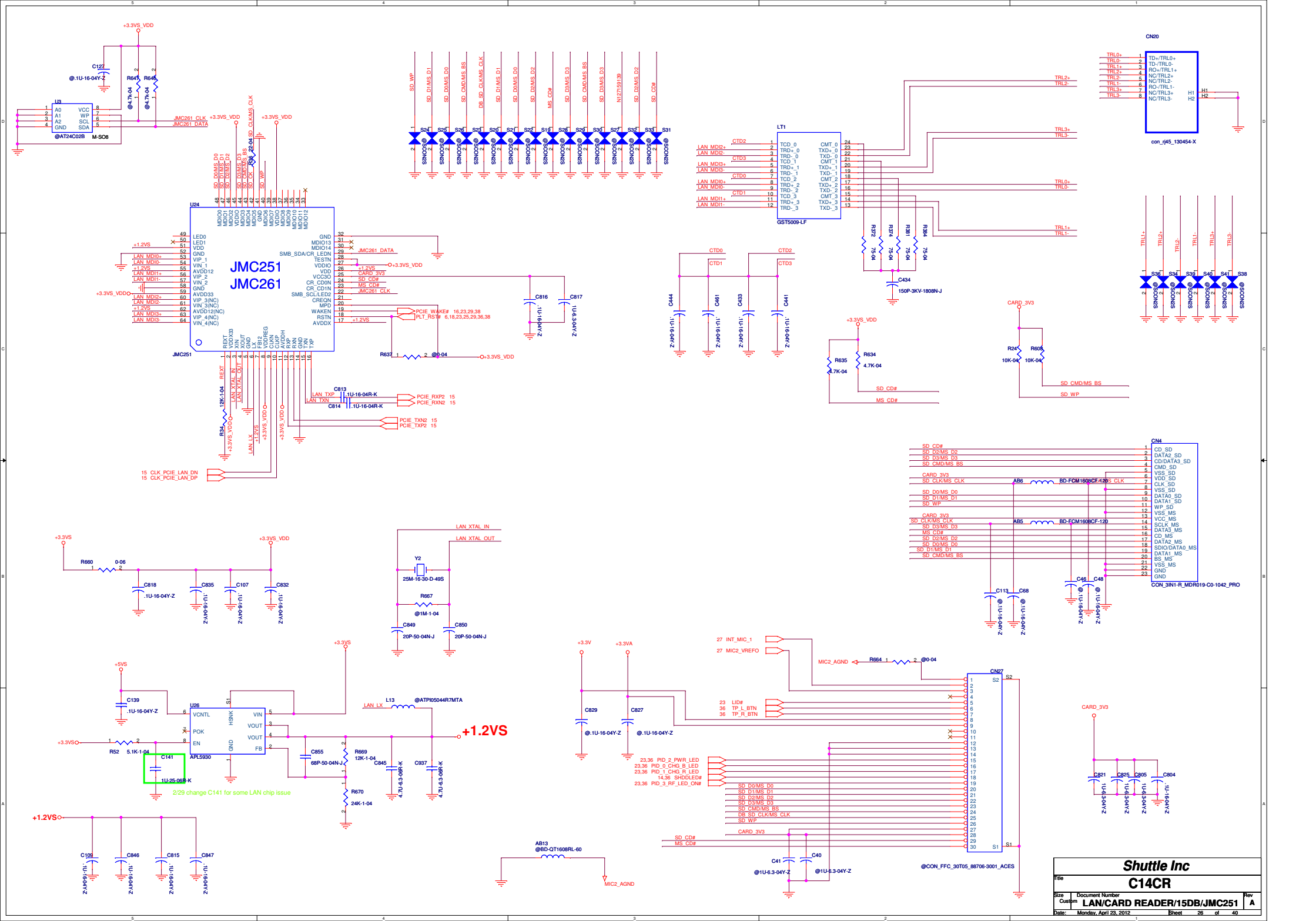
CRT CONN

LVDS CONN

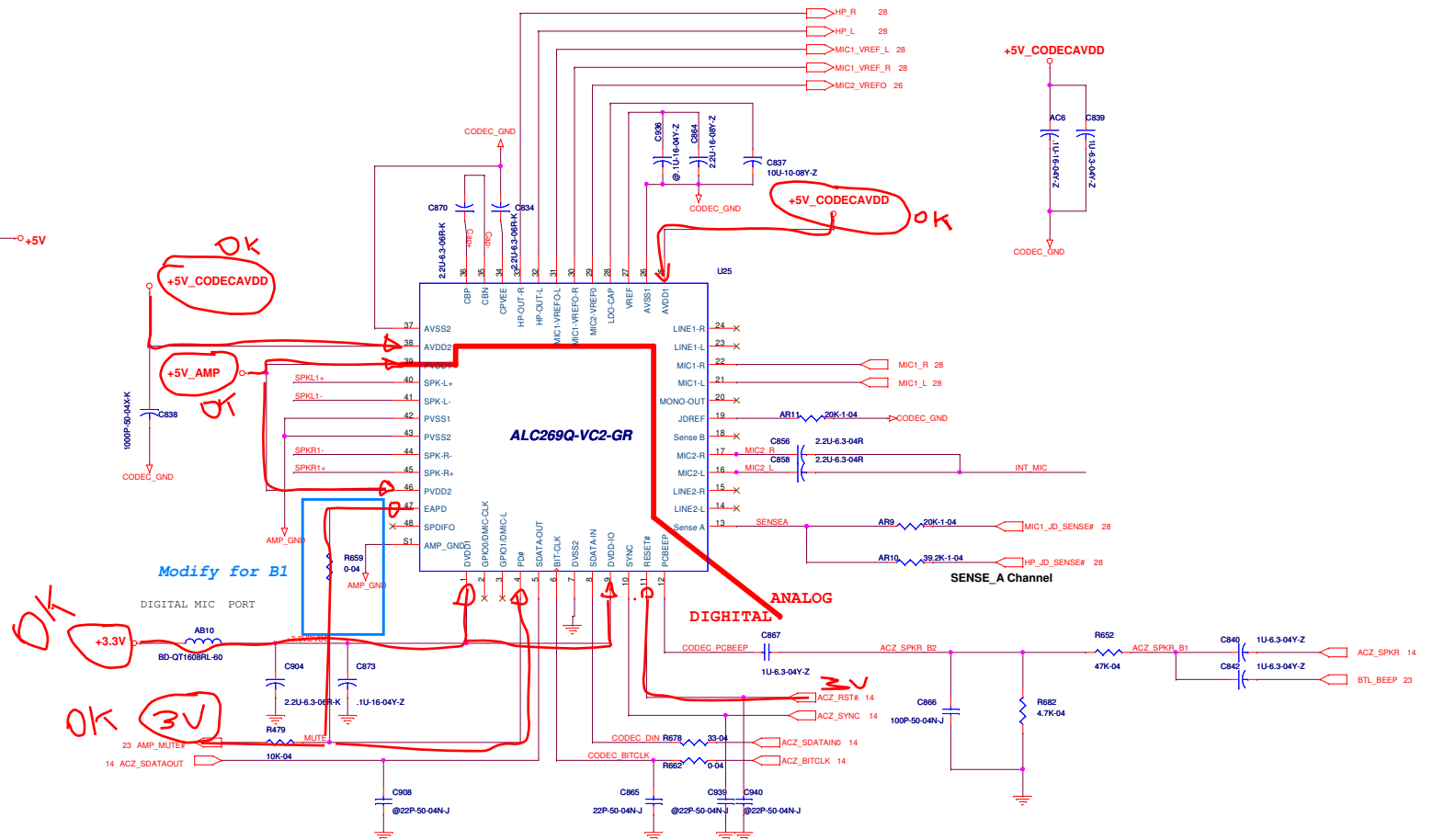
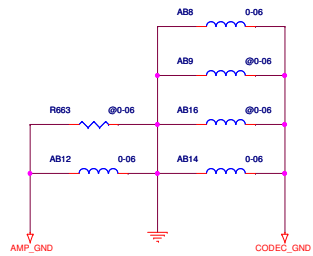


PWR SW





AMP VDD



環景球唱1.6A

SPKR1+ AB1 BQ-QT1608RL-60

SPKR1- AB2 BQ-QT1608RL-60

SPKL1- AB3 BQ-QT1608RL-60

SPKL1+ AB4 BQ-QT1608RL-60

T21 QT1608RL 120HC-3A

ACN1

SPKR_R+ 1

SPKR_L 2

SPKL_L 3

SPKR_L+ 4

S1

S2

CON_WB-4V125_B5205-04001_ACES

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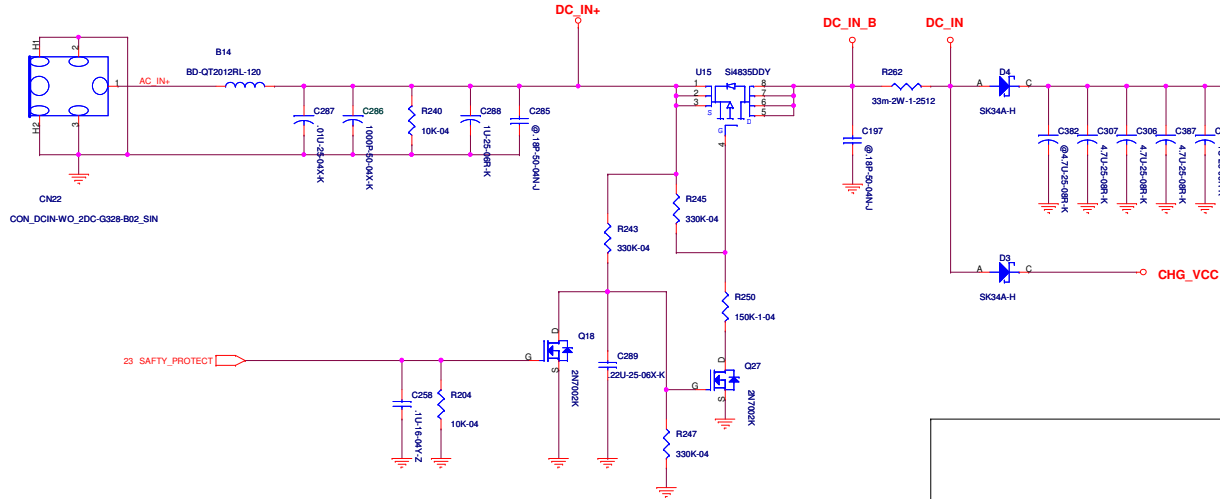
426

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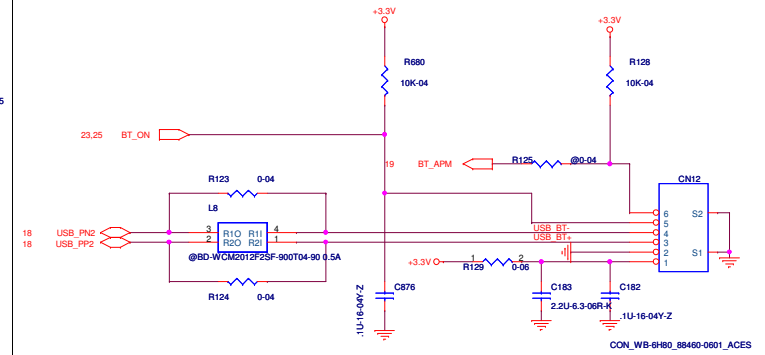
[illegible]

DC IN

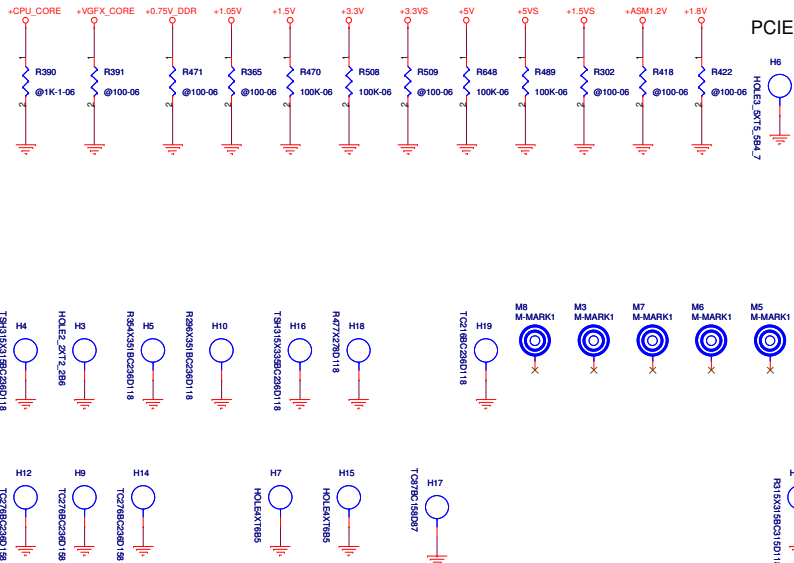
PROJECT	C14CR03		
Adaptor	65W	90W	120W
Rsense	33m Ohm	25m Ohm	18m Ohm
Stop Charger	60W	80W	110W



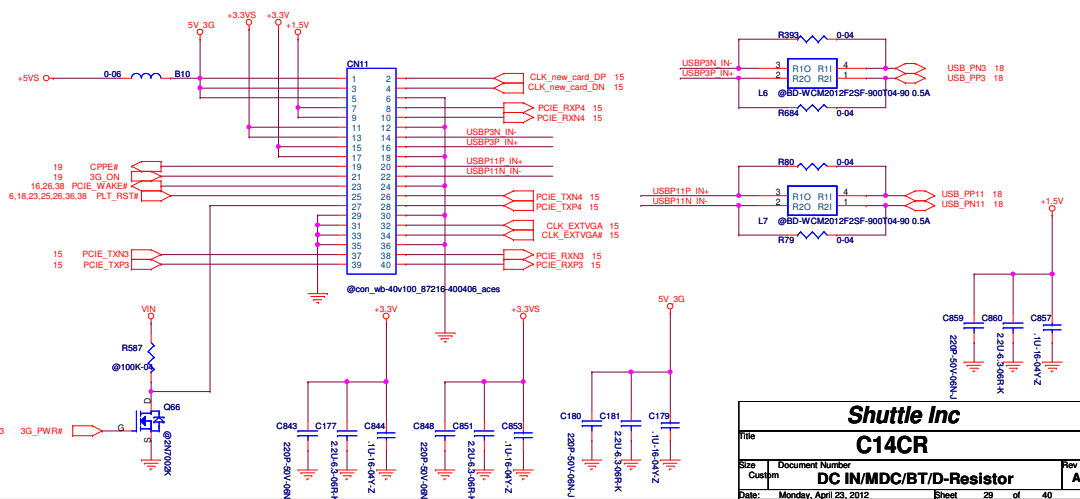
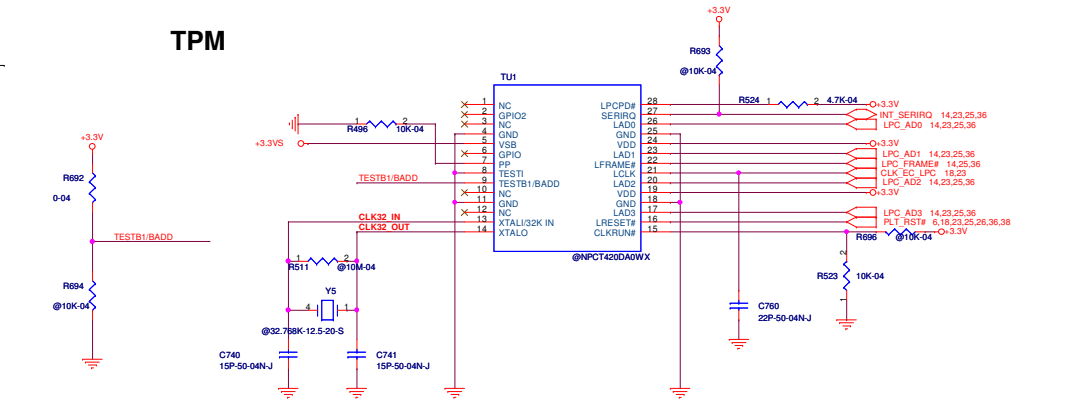
BT CONN



Discharge Resistor

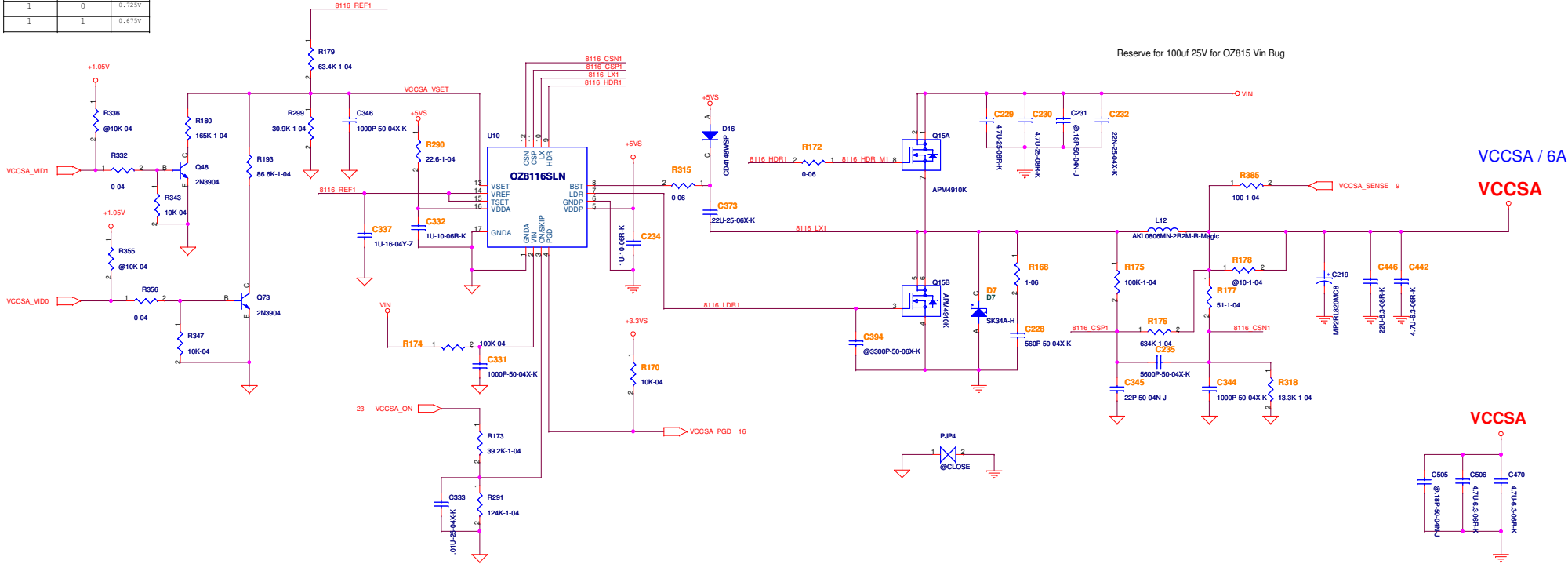


TPM



Shuttle Inc		
C14CR		
Size	Document Number	Rev
Custom	DC IN/MDC/BT/D-Resistor	A
Date:	Monday, April 23, 2012	Sheet 29 of 40

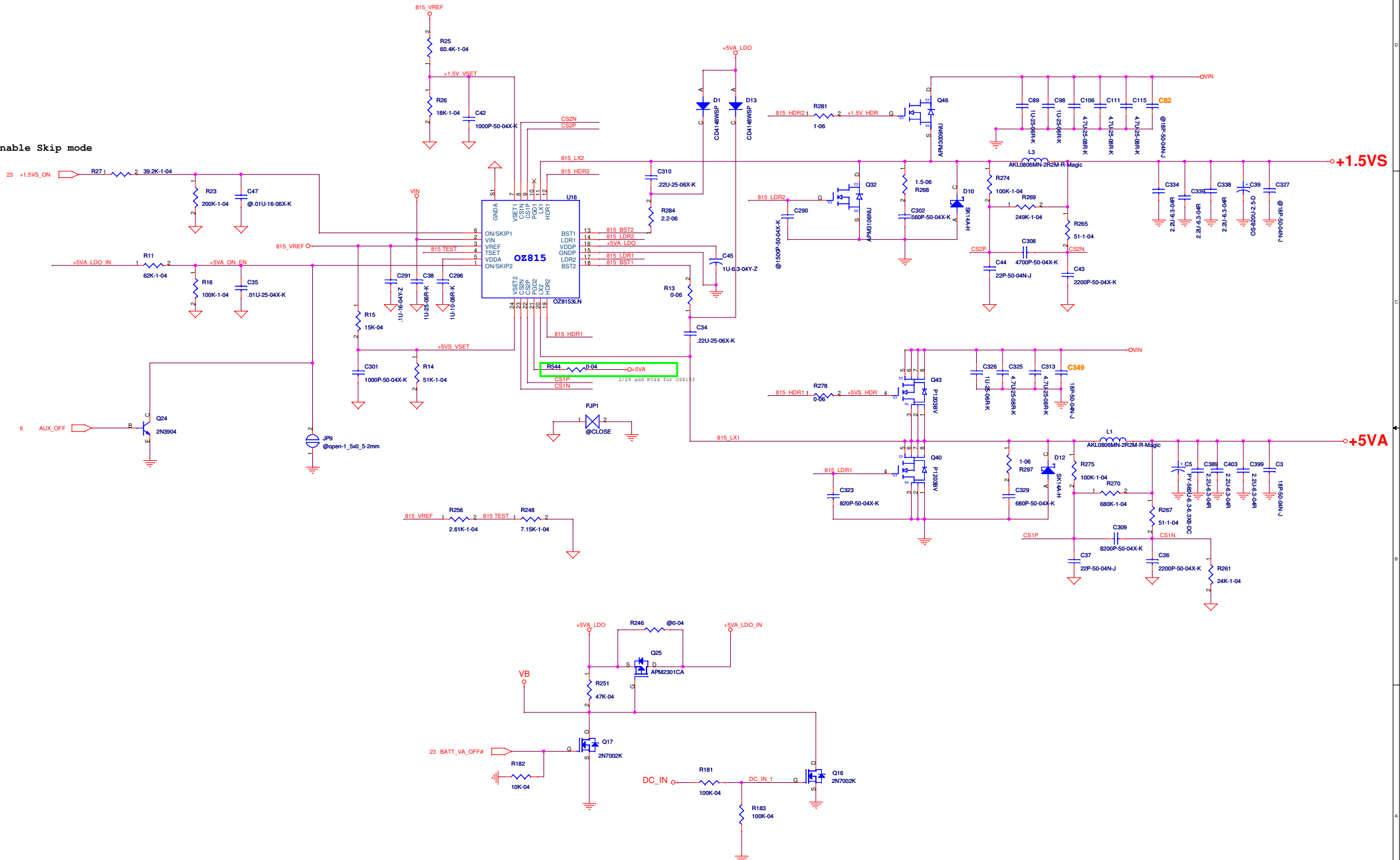
VCCSA_SEL		
VCCSA_VID0	VCCSA_VID1	V_set
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



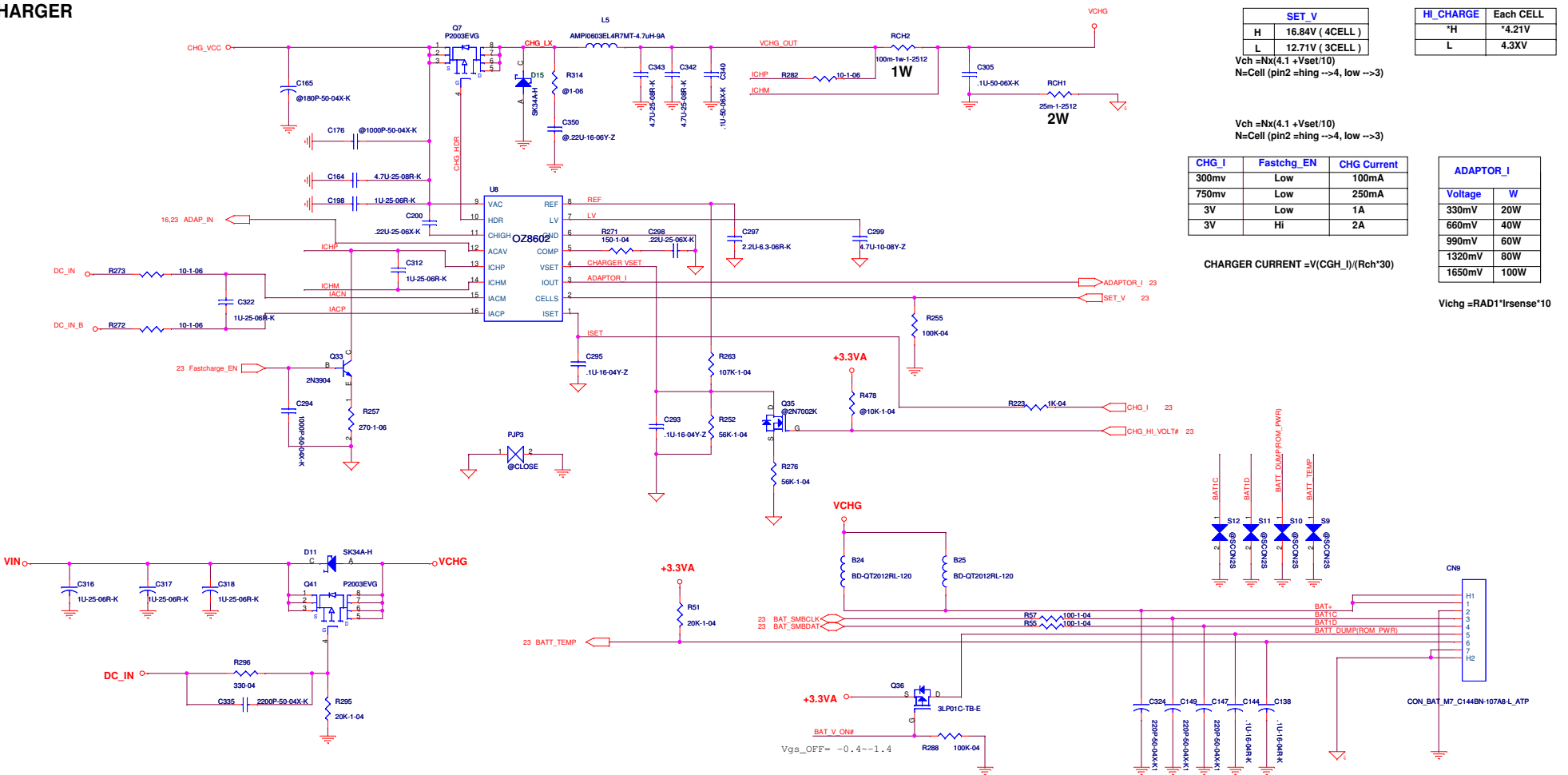
+1.8V/+5V_ON Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

$$\text{Output Voltage} = \left[\text{Vref} \times \frac{R2}{(R1+R2)} \right] \times 2$$

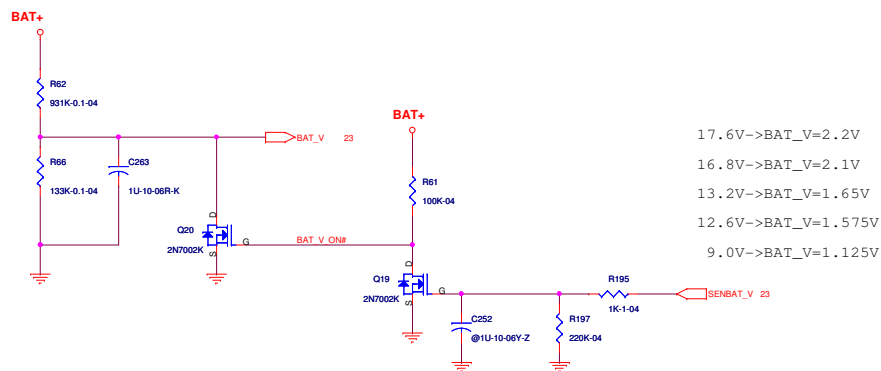
Enable Skip mode



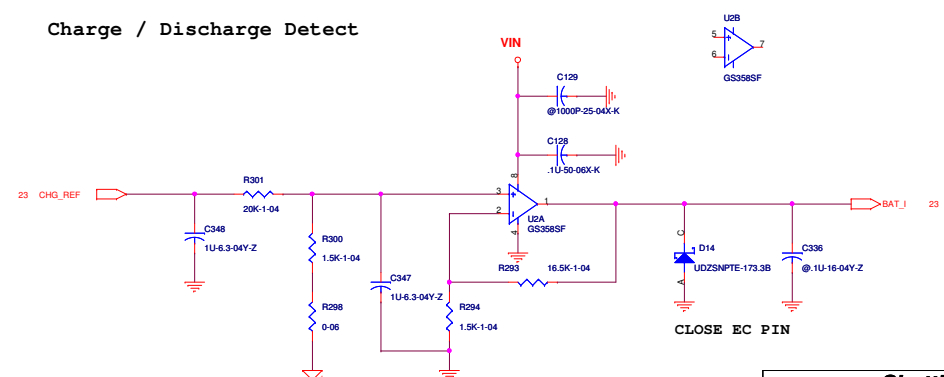
CHARGER

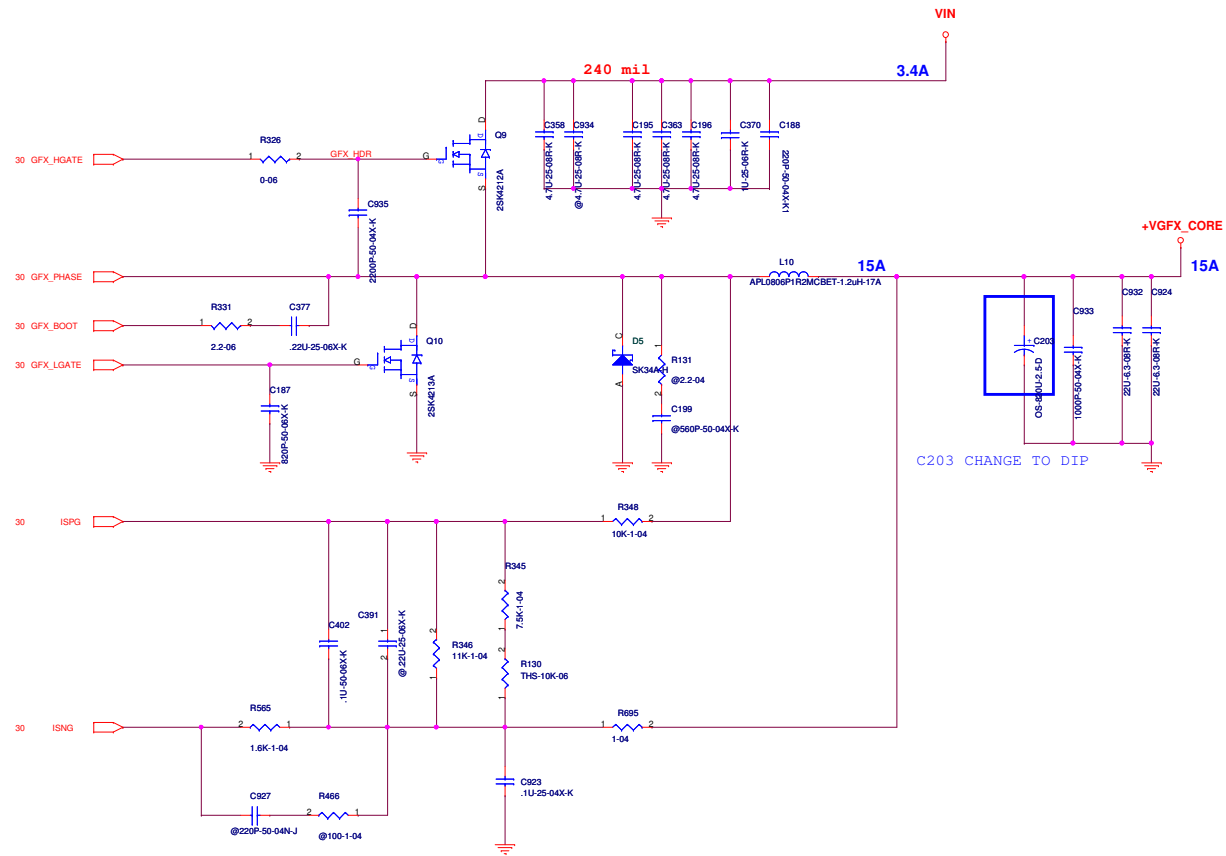
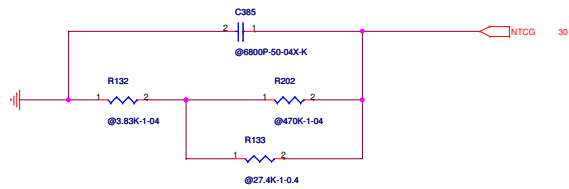


Battery Voltage Detect

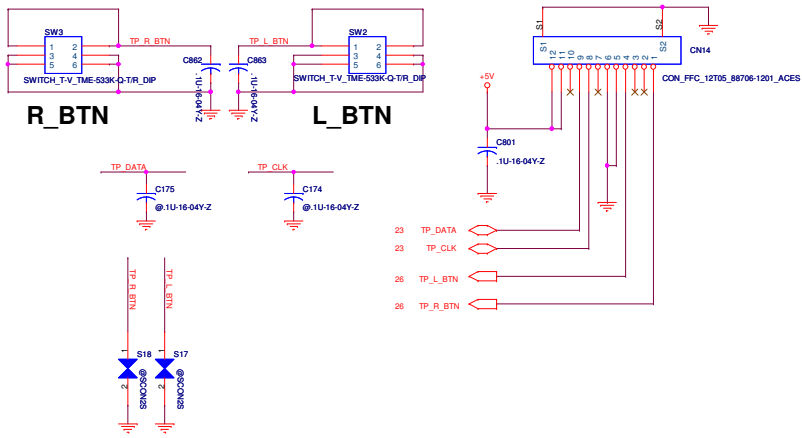


Charge / Discharge Detect

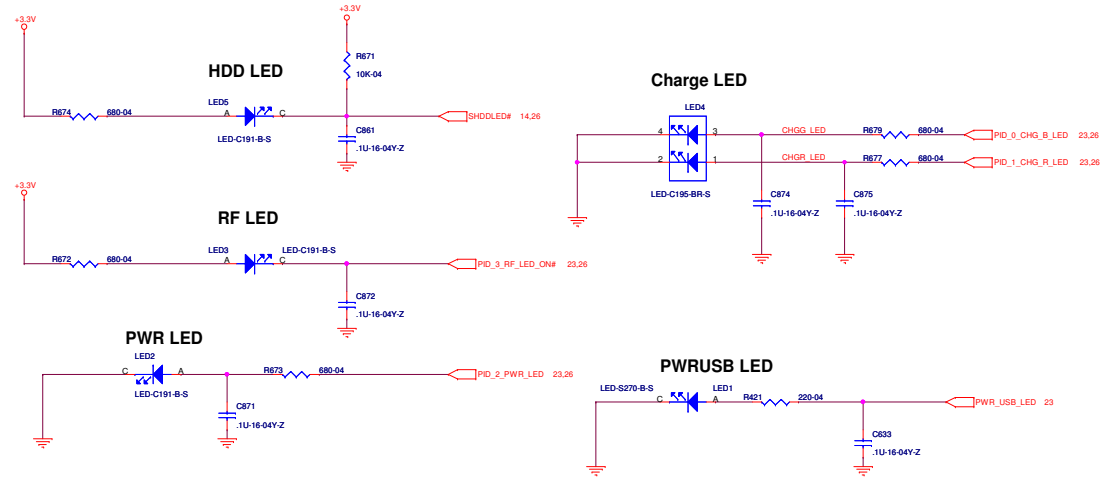




Touch Pad

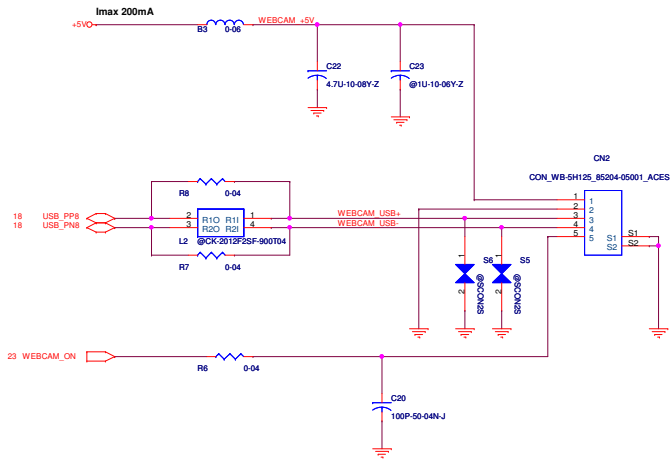


LED

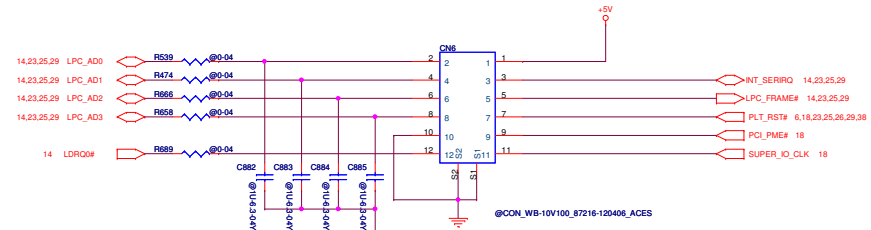


Webcam CONN

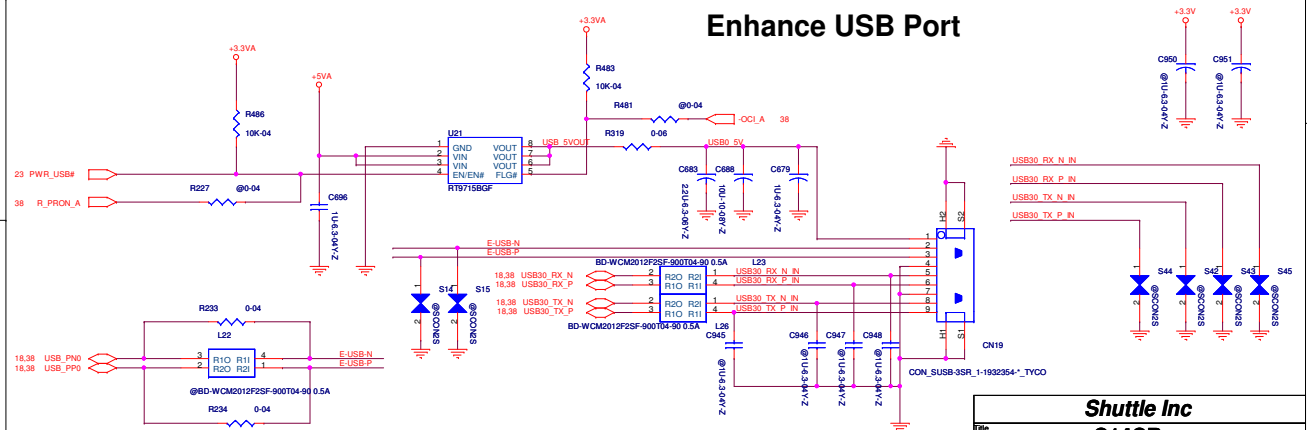
WEBCAM_ON	
1	ON
0	OFF



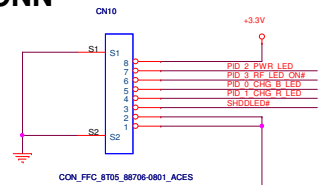
RS232 CONN



Enhance USB Port



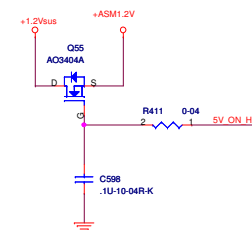
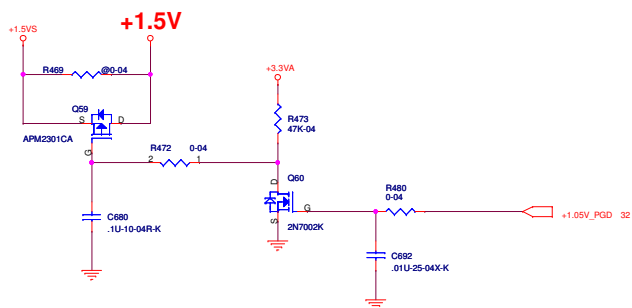
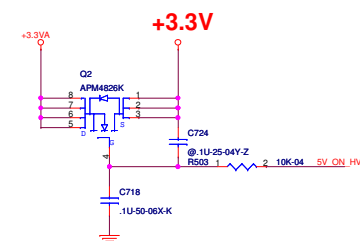
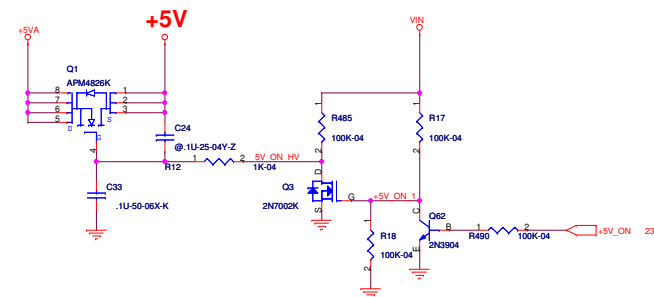
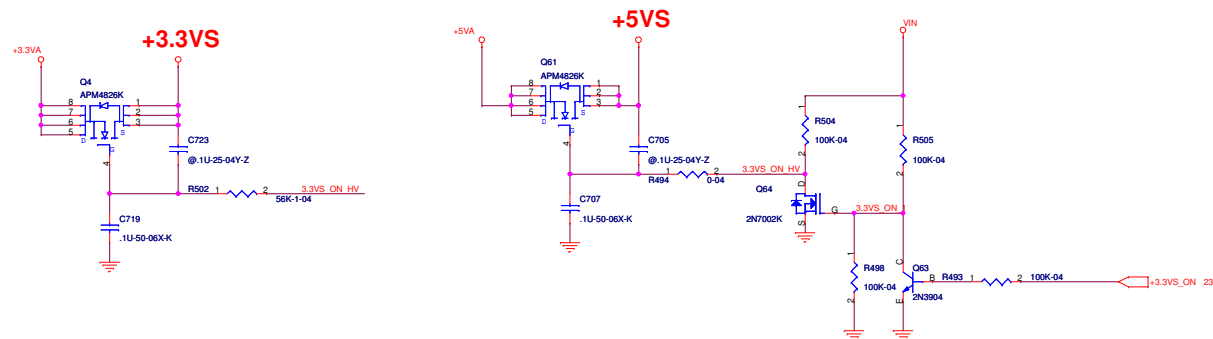
LED CONN



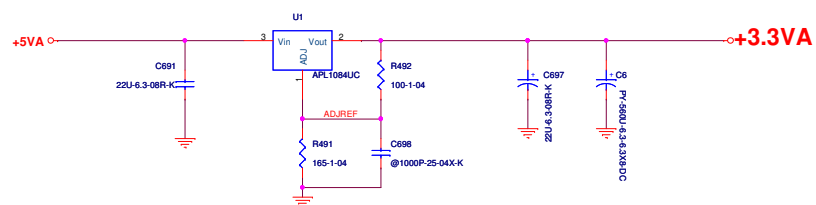
Shuttle Inc
C14CR

File	Document Number	Rev
Size	Custom	TP/LED/WEBCAM/USB CHARGER A
Date	Monday, April 23, 2012	Sheet 36 of 40

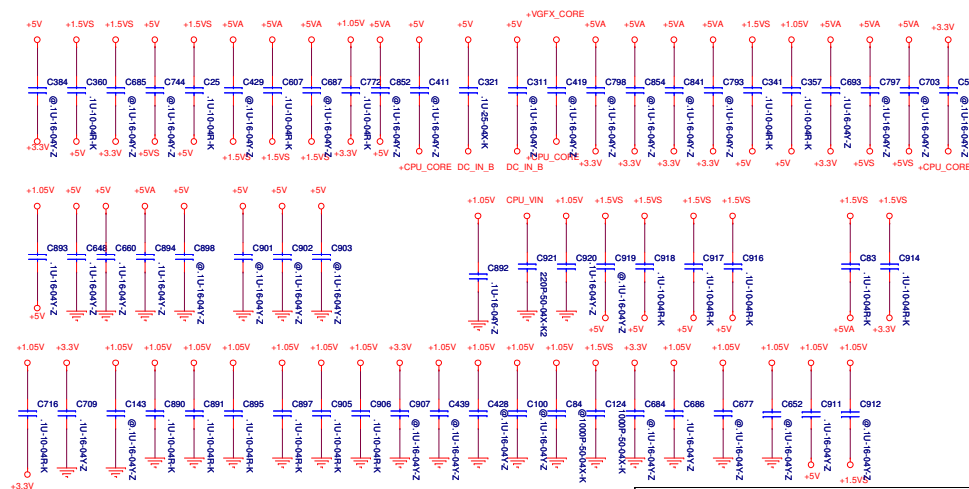
VCCSW



LDO

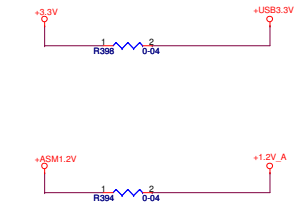


HIGH-SPEED CAP



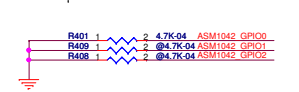
<div style="text-align: right;">+1.5VS*</div> <h1 style="text-align: center;">Shuttle Inc</h1>			
Title <h2 style="text-align: center;">C14CR</h2>			
Size Custom	Document Number <h3 style="text-align: center;">VCC SW/+3.3VA/HIGH-SPEED CAP</h3>		Rev A
Date:	Monday, April 23, 2012	Sheet	37 of 40

USB 3.0

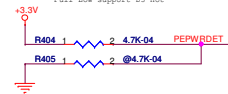


GPIO0	GPIO1	GPIO2	Function
1	1	0	Synchronous Mode
1	1	1	Asynchronous Mode (default)
0	0	x	Debug/Test Mode

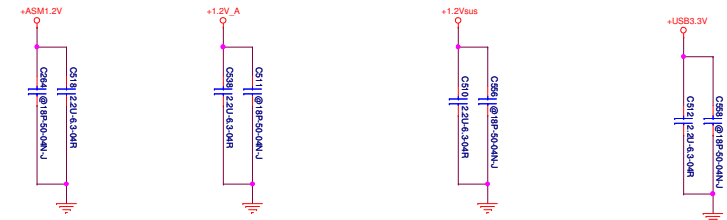
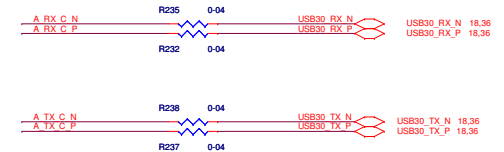
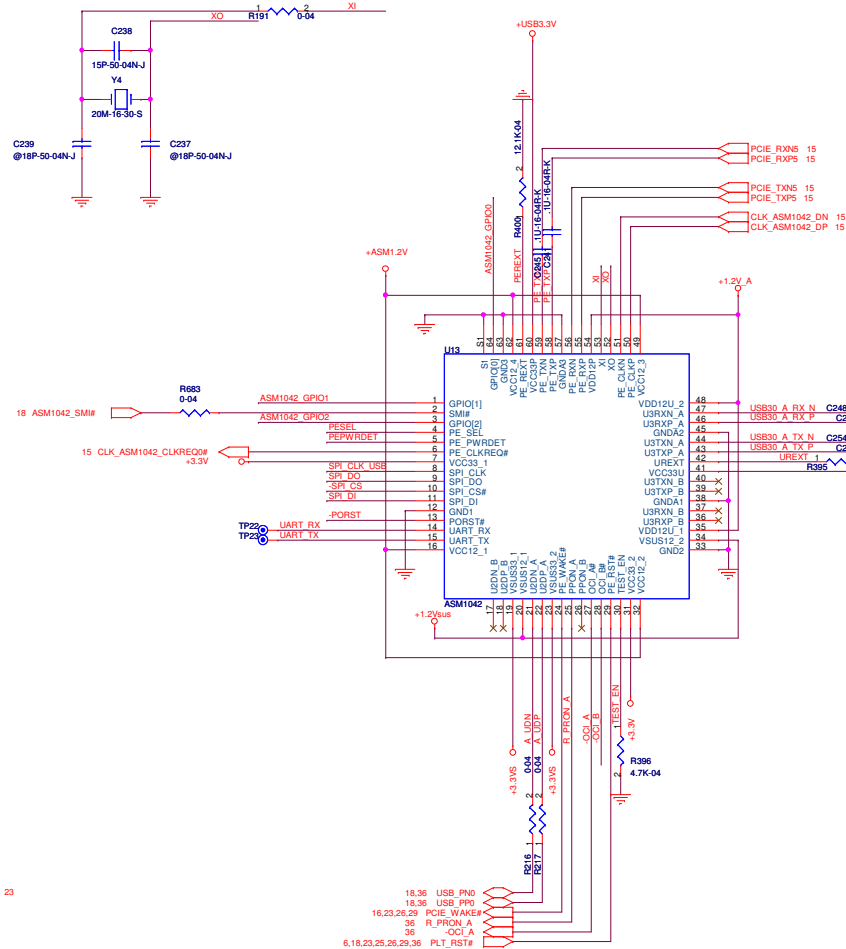
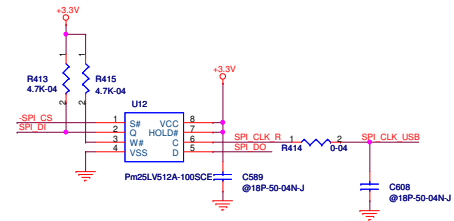
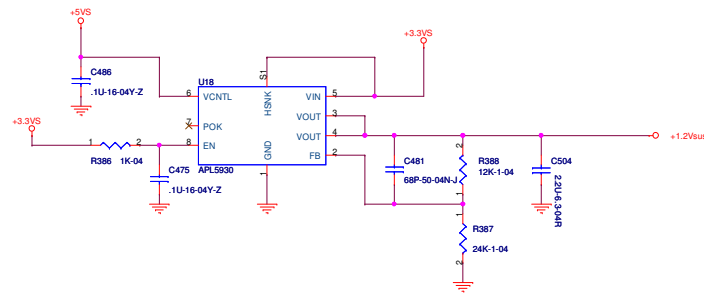
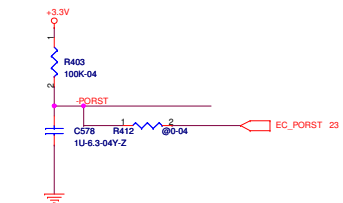
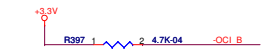
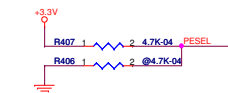
* GPIO0 GPIO1 GPIO2 internal Pull-high



```
PEFWRDET
PCI Express Remote/Wakeup Indicator
Pull-high support D3 Cold
Pull-Low support D3 Hot
```



PESEL
Pull-high for others application
Pull-Low for Express Card/Mini card appliaction



MA1:Change net name from PCH_SMB_CLK to PCH_SMB_CLK_DDR
MA2:Change net name from PCH_SMB_DATA to PCH_SMB_DATA_DDR
MA3:DEL CLK_ASM1042_CLKREQ0# path(R87 OP)
MA4:Change ACPRESENT to EC pin 88
MA5:ADD OR FOR 25MHZ CLK(R534)
MA6:ADD OR FOR PCH SATA POWER(B6)
MA7:Sharing System BIOS ROM for KB & EC Codes(Del U7)
MA8:ADD EC_HSCK path for sharing ROM(ADD R540)
MA9:ADD EC_HSCS0# path for sharing ROM(ADD R484)
MA10:ADD EC_HMOSI path for sharing ROM(ADD R212)
MA11:ADD EC_HMISO path for sharing ROM(ADD R482)
MA12:ADD OR FOR AMP_GND(ADD AB12)
MA13:Change CN16 PIN DEFINE
MA14:DEL R147 for PROCHOT issue
MA15:ADD ISEN1 Pull Hi +5V(ADD R356)
MA16:Change C203 SMD CAP TO DIP CAP
MA17:ADD ASM1042_SMI# path(ADD R683)
MA18:Change CN19 PIN DEFINE
MA19:ADD EMI solution(ADD C251,C257,C357,C341,C684,C686,C25,C660,C677 DEL C99,C430)

MB1:Change CPURST# path(OP:R457,Q72,R656,Q71,R659 ADD:R452,R453)
MB2:Change DDR3_DRAMRST_R path(OP:Q67 ADD:R628)
MB3:Change PM_SYSRST# Pull_up power to +3.3V
MB4:Change USB part 1(External USB)to USB part 12 for testingSignal
MB5:Sharing System BIOS ROM for KB & EC Codes(OP:R110,R531,R107,R94)
MB6:ADD SYS_TEMP EC Pin68 for Thermal(ADD RT1,R426)
MB7:ADD CPU Thermal Sensor NTC7717U for Thermal(ADD U27,R693,C887)
MB8:Change SATA3RBIAS external pull-down resistor for testingSignal (R90:1K-1-04)
MB9:ADD RS-232 CONNECT FOR DA18(OP:CN6,,R539,R474,R666,R658,R689,C882,C883,C884,C885)
MB10:Change ASM1042_SMI# path for AMI(GPIO4)

V1.0 1:Change R417 resistor 0R
V1.0 2:Add R400,R395 resistor for BOM issue
V1.0 3:Change R403 resistor 100K for USB3.0 power sequence
V1.0 4:Add R193,C585,R171,C416 place for ISL95831 IC
V1.0 5:ADD EMI solution(OP:C430,C428,C912,C652,C677,C327,C368,C369,C82,C778,C795,C153,C146,C722 Add:C251,C257,C357,C341,C25,AB8.AB9,C360,C83,C917,C879,C188,C916,C607,C918,C914,C772,C716,C321,C758,C746)

- 1. 10/10 connect SM_VREF(page 09) to DIMM pin 126(page 12,13)
- 2. 10/10 R360 R361 placement, R323 R416 OP (page12,13)
- 3. 10/10 R433 mount, R437 OP(page 23)
- 4. 10/10 change CRT HSYNC & VSYNC FET to gate, change C279, C280 from 10p to 15p (page 24).
- 5. 10/11 A,B phase Power input & output add jump, convenient for power measurement & debug
- 6. 10/11 VCCSA power R178 unmount
- 7. 10/11 1.05V power R337unmount. disable VCCIO 1.0V, reserve the other circuit.
- 8. 10/20 C693 C894 placement for ESD issue (page 37)
- 9. 10/21 separate connect MIC1_VREF_L & MIC1_VREF_R to MIC1_L & MIC1_R (page 28)
- 10. 10/21 add C928 C831 & AR7 AR8. (page 28)
- 11. 10/21 change CPU core.IGPU core to ISL95831
- 12. 10/21 R352 R354 change to capacitor (C929 C930)
- 12. 10/22 Cancel JP11,JP12,JP13,JP14
- 13. 10/22 placement C709
- 14. 10/21 placement C730 C732 C735 C745 close to connector
- 15. 11/07 change platform ID, R433 OP and R437 placement

B Phase

- 16. 11/30 EMI change R218 to B28, R589 to B29, change value for R662,L24,L25,AR1 , add C938.
- 17. 11/30 internal USB3.0 change value for C248,C250,C254,C256, mount R481, R401.
- 18. 11/30 internal USB3.0 add R352,R354
- 19. 11/30 CRT add Q56,Q22 for colay; U28,U29 unmount; change value for R551.
- 20. 11/30 flash ROM OP R120,R121,R127,C185.
- 21. 11/30 VCCSA change C362,C380 to R343,R347; OP R336,R355; change value for R332,R356,R385.
- 22. 11/30 1.05V OP: Q62,Q50,Q49,R328,R320,R344,R376,C443,C536,C599,R370.
- 23. 11/30 CPU_CORE OP C527,C562,C594,C225; add C362.
- 24. 11/30 LAN add C937,L13.
- 25. 11/30 USB add R89,R95,R203,R205.
- 26. 11/30 OP 0 ohm resistor: R442,R521,R693,R594,R592,R526,R591,R705,R656,R514,R116,R687,R532,R527,R621,R544,R630,R279,R35,R636,R382,R383,R373,R154,R155,R665,R201,R558,
- 27. 11/30 audio change value for U25,AR3,AR4; OP: C908,AB7; mount AC7,AB15,AB8; add C941,C942.
- 28. 11/30 add TPM, finger print, Express card component.
- 29. 12/02 SATA change value for R537.

12/06 done

C Phase

- 30. 2/29 add R544 connect to SVA for OZ8153
- 31. 2/29 connect +VCCPLLVRM with page 20 and page 21
- 32. 2/29 add WOL, (connect LAN wake on to EC).
- 33. 3/2 Del SW5, add JP9
- 34. USB co-lay add R279, R287, R211, R218, R316, R373
- 35. 4/9 Del JP point and add R591,R592 for new combo card
- 36. 4/19 change W/LAN 3G_PWR# to BT_ON.

Shuttle Inc			
C14CR			
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